PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Jiang et al.

Serial No.: 09/483,712

Filed: January 14, 2000

For: INTERMEDIATE STRUCTURES FOR CHIP-SCALE PACKAGES HAVING CARRIER BONDS (as amended)

Confirmation No.: 8743

Examiner: M. Warren

Group Art Unit: 2815

Attorney Docket No.: 2269-3815.1US
(98-0670.00/US)

VIA ELECTRONIC FILING
AUGUST 25, 2008

AMENDED APPEAL BRIEF

Mail Stop Appeal Brief – Patent
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sirs:

This Amended Appeal Brief is being submitted in response to the Notification of Non-Compliant Appeal Brief mailed July 25, 2008, and is intended to replace the Appeal Brief filed March 7, 2007. This Amended Appeal Brief includes revisions to Section 2 (Related Appeals and Interferences), Section 5 (Summary of the Claimed Subject Mater), and Section 10 (Related

Proceedings Appendix), but is otherwise identical to the Appeal Brief filed March 7, 2007. Appellants further reaffirm the arguments set forth in the Reply Brief filed September 10, 2007.

1) REAL PARTY IN INTEREST

The real party in interest in the present pending appeal is Micron Technology, Inc., Assignee of the pending application as recorded with the United States Patent and Trademark Office on January 14, 2000, at Reel 010532, Frame 0640.

2) RELATED APPEALS AND INTERFERENCES

An appeal was previously filed in this application (Appeal No. 2004-2144), and a Decision on Appeal was mailed on November 19, 2004 in which the Examiner's then standing rejections were affirmed. A copy of the Decision on Appeal issued November 19, 2004 is attached hereto in a "Related Proceedings Appendix." The Appellants, the Appellants' representative, and the Assignee are not aware of any other prior or pending appeal, judicial proceeding, or interference that would relate to, directly affect, be directly affected by, or have a bearing on the Board's decision in the pending appeal.

3) STATUS OF THE CLAIMS

Claims 1 through 16 and 19 are pending in the application.

Claims 17, 18, and 20 through 29 are canceled.

Claims 1 through 16 and 19 stand rejected.

No claims are allowed.

Claims 1 through 16 and 19 are the subject of the pending appeal.

4) STATUS OF AMENDMENTS

No amendments have been filed subsequent to the Final Office Action mailed September 6, 2006.

5) SUMMARY OF THE CLAIMED SUBJECT MATTER

The presently claimed invention is directed to intermediate structures formed during fabrication of so-called "chip-scale packages," such as the embodiments of the chip-scale package 100 shown in Figures 2 through 6 of the as-filed application for the present invention (hereinafter "the Application"), which are a type of semiconductor device.

In particular, the claimed invention in the present application is an intermediate structure formed during fabrication of a chip-scale package that includes a semiconductor die 10 having at least one bond pad 12 on an active surface 11 of the semiconductor die 10. The Application, Page 6, Lines 14-26; Figures 2-5. At least one discrete conductive bond 16, 40 connects an end of a conductive lead frame member 14, 20 to the at least one bond pad 12. Id. at Page 6, Lines 14-15; page 8, lines 7-15; Figures 2-5. At least one carrier bond 18, 50 is attached to an upper surface of the conductive lead frame member 14, 20 and extends transversely thereto. Id. at Page 6, Line 26 – Page 7, Line 2; Page 7, Lines 19-21; Page 8, Lines 16-24; Figures 2-5. Also, the intermediate structure is free of encapsulant material 60 that is to be subsequently applied to the

intermediate structure to form the chip-scale package 100. Id., Page 9, Lines 4-14; Page 10, Lines 15-21. In some embodiments, the carrier bonds 18, 50 comprise a conductive or conductor-filled epoxy material. The Application, Page 5, Lines 6-8; Page 8, Lines 19-23; Claim 14. Claim charts for each of independent claims 1 and 2 are set forth below, which maps the elements and limitations recited in the claims to the specification.

Independent Claim 1	
An intermediate structure in the fabrication of a chip-scale package comprising:	
a semiconductor die having an active surface having at least one bond pad thereon, sides and a back side;	Page 6, Line 14; Page 7, Lines 4-11; Figures 2-5
at least one conductive lead frame member laterally spaced from the at least one bond pad and having an upper surface and a lower surface,	Page 6, Lines 14-15; Page 6, Lines 22-23; Page 7, Lines 12-19; Figures 2-5
the lower surface of the at least one conductive lead frame member having and inner end and an outer end and being substantially non-conductively attached to a portion of the active surface of the semiconductor die and vertically spaced therefrom by a non-coextensive dielectric element interposed therebetween;	Page 6, Lines 22-26; Page 7, Lines 22-28; Figures 2-5; Page 10, Lines 4-7; Figures 2-5
at least one discrete conductive bond connecting the inner end of the at least one conductive lead frame member to the at least one bond pad on the active surface of the semiconductor die;	Page 6, Lines 14-16; Page 7, Lines 5-6; Page 8, Lines 7-15; Page 10, Lines 7-9; Figures 2-6
at least one carrier bond directly attached to the upper surface of the at least one conductive lead frame member at the outer end thereof and extending transversely thereto; and	Page 6, Lines 16-19; Page 6, Line 26 – Page 7, Line 2; Page 7, Lines 19-21; Page 8, Lines 16-24; Page 8, Lines 27-29; Page 10, Lines 9-10; Figures 2-5
wherein the intermediate structure is free of an encapsulant material to be subsequently applied to the intermediate structure.	Page 9, Lines 4-14; Page 10, Lines 15-21

Independent Claim 2	
An intermediate structure in the fabrication of a chip-scale package comprising:	
a semiconductor die having an active surface having a plurality of bond pads thereon;	Page 6, Line 14; Page 7, Lines 4-11; Figures 2-5
a dielectric element having an upper surface and a lower surface, the lower surface of the dielectric element attached to a portion of the active surface of the semiconductor die;	Page 6, Lines 22-26; Page 7, Lines 22-28; Figures 2-5; Page 10, Lines 4-7; Figures 2-5
a plurality of conductive lead frame members having inner ends laterally spaced from the plurality of bond pads, each conductive lead frame member of the plurality of conductive lead frame members having an upper surface and a lower surface,	Page 6, Lines 14-15; Page 6, Lines 22-23; Page 7, Lines 12-19; Figures 2-5
a portion of the lower surface of each conductive lead frame member of the plurality of conductive lead frame members being attached to a portion of the upper surface of the dielectric element for connecting each conductive lead frame member of the plurality of conductive lead frame members to the active surface of the semiconductor die;	Page 6, Lines 22-26; Page 7, Lines 22-28; Figures 2-5; Page 10, Lines 4-7; Figures 2-5
a plurality of discrete conductive bond members, at least one discrete conductive bond member of the plurality of conductive bond members connecting the inner end of each conductive lead frame member of the plurality of conductive lead frame members to at least one bond pad of the plurality of bond pads on the active surface of the semiconductor die;	Page 6, Lines 14-16; Page 7, Lines 5-6; Page 8, Lines 7-15; Page 10, Lines 7-9; Figures 2-6
a plurality of conductive carrier bonds, at least one carrier bond of the plurality of conductive carrier bonds directly disposed on the upper surface of each conductive lead frame member of the plurality of conductive lead frame members at a location remote from the inner end thereof and extending transversely from the upper surface thereof; and	Page 6, Lines 16-19; Page 6, Line 26 – Page 7, Line 2; Page 7, Lines 19-21; Page 8, Lines 16-24; Page 8, Lines 27-29; Page 10, Lines 9-10; Figures 2-5

wherein the intermediate structure is free of an encapsulant material to be subsequently applied to the intermediate structure.	Page 9, Lines 4-14; Page 10, Lines 15-21

6) GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

(A) The First Rejection

Appellants request that the Board review the rejection of Claims 1, 2, 5 through 9, 13 through 16, and 19 under 35 U.S.C. § 103(a) as being unpatentable over United States Patent No. 5,677,566 to King et al. (hereinafter "King et al.") in view of United States Patent Application Publication No. 2001/0011773 A1, filed by Havens et al (hereinafter "Havens et al."), which was made in a Final Office Action mailed September 6, 2006 (hereinafter "the Final Action").

(B) The Second Rejection

Appellants additionally request that the Board review the rejection of Claims 3, 4, and 10 through 12 under 35 U.S.C. § 103(a) as being unpatentable over King et al. and Havens et al. in further view of United States Patent No. 5,894,107 to Lee et al. (hereinafter "Lee et al."), which also was made in the Final Office Action.

7) ARGUMENT

(A) The First Rejection

(i) Claims 1, 2, 5-9, 13, 15, 16, and 19

Appellants assert that the U.S. Patent and Trademark Office (the "Office") has failed to establish a *prima facie* case of obviousness with respect to Claims 1, 2, 5 through 9, 13, 15, 16,

and 19 because the Office has failed to identify a sufficient motivation to combine the teachings of King et al. with the teachings of Havens et al. in the manner proposed by the Office.

Rejection of claims under 35 U.S.C. § 103(a) requires that the Office establish a *prima facie* case of obviousness. M.P.E.P. § 2142. M.P.E.P. 706.02(j) sets forth the standard for an obviousness rejection:

> To establish a *prima facie* case of obviousness, three basic criteria must be met. **First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings.** Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

To provide a motivation or suggestion to combine, the prior art or the knowledge of a person of ordinary skill in the art must "suggest the desirability of the combination" or provide "an objective reason to combine the teachings of the references." M.P.E.P. § 2143.01. It is improper to combine references where the references teach away from combination. M.P.E.P. § 2145.

Appellants admit that King et al. teaches a final chip-scale package substantially similar to the final chip-scale package taught in the application for the present invention. Appellants and the Office appear to agree, however, that King et al. teaches (with respect to Figures 4 through 8 therein) a method of manufacturing the chip-scale package in which the carrier bonds are attached to the conductive leads after encapsulation, but does not teach or suggest a method in which the carrier bonds are attached to the conductive leads prior to encapsulation, as taught at

Page 9, lines 4 through 14 of the Application for the present invention. As such, Appellants and the Office further appear to agree that King et al. does not teach or suggest an intermediate structure as claimed in either of independent Claims 1 and 2, in which at least one carrier bond is directly attached to (Claim 1) or disposed on (Claim 2) the upper surface of at least one conductive lead frame member of the intermediate structure, and the intermediate structure is free of an encapsulant material.

The Office has asserted that although King et al. does not teach such as intermediate structure, one of ordinary skill in the art, considering King et al. in view of Havens et al., would have been motivated to combine the teachings of Havens et al. with the teachings of King et al. in such a way as to provide an intermediate structure as recited in each of independent Claims 1 and 2. Appellants respectfully disagree for the reasons set forth below.

Havens et al. teaches a hydrophobic hermetic covering that can be applied to substantially all external surfaces of an electronic package, and methods of applying the hydrophobic hermetic covering to external surfaces of an electronic package. Havens et al., Page 2, Paragraph [0025]. Havens et al. teaches that the hermetic covering may comprise a thin layer (e.g., 0.001 inches) of Teflon® material or another fluorinated thermoset material. Id., Page 3, Paragraphs [0031], [0033], [0037].

Havens et al. teaches that carrier bonds (e.g., solder balls 6) can be applied to a substrate 3 of an electronic package 1 before applying the hydrophobic hermetic covering to the package 1 (Havens et al., Page 2, Paragraph [0028] – Page 3, Paragraph [0031]), or after applying the hydrophobic hermetic covering to the package 1 (Id., Page 5, Paragraphs [0057]-[0058]).

Appellants admit that one of ordinary skill in the art, considering the combined teachings of King et al. and Havens et al. as a whole at the time the present invention was made, may have been motivated to replace the encapsulating material 26 of the device taught by King et al. (See e.g., King et al., column 3, lines 28-33) with a hermetic covering as taught in Havens et al. to address the moisture sensitivity problem addressed by Havens et al. (See e.g., Havens et al., Page 1, Paragraphs [0002]-[0003]; Page 2, Paragraph [0025]). Appellants respectfully assert, however, that in so doing, one of ordinary skill in the art would have been motivated to attach the carrier bonds to the conductive leads of the device taught by King et al. *after* applying the hermetic covering, and *not before*, as asserted by the Office.

As previously mentioned, King et al. teaches attaching the carrier bonds (external electrodes 28) after applying the encapsulating material. King et al., Column 4, Lines 35-65. Havens et al. also teaches that the carrier bonds (solder balls 6) may be attached after applying the hermetic covering to the package. As a result, this method is in accordance with both the teachings of King et al. and Havens et al., and as such, clearly would have been the obvious method of choice to one of ordinary skill in the art at the time the present invention was made. While Havens et al. teaches that the carrier bonds 6 may be attached to the electronic package 1 either before or after applying the hermetic covering, there is no reason one of ordinary skill in the art would be motivated to further and unnecessarily modify the teachings of King et al. so as to attach the carrier bonds before applying the hermetic covering. In other words, the prior art references do not teach or suggest the desirability of attaching the carrier bonds before applying

the hermetic covering as opposed to attaching the carrier bonds after applying the hermetic covering.

The Office appears to assert at Pages 6-7 of the outstanding Office Action that Havens et al. teaches that attaching the carrier bonds to the conductive leads of the device taught therein before applying the hermetic covering would improve reliability and product yield, and hence, one of ordinary skill in the art would have been motivated at the time the present invention was made to attach the carrier bonds to the conductive leads of the device taught therein after applying the hermetic covering of Havens et al. to the structure of King et al. to improve reliability and product yield. Appellants note, however, that Havens et al. teaches that the invention taught therein "largely solves the moisture sensitivity problem associated with electronic packages by covering substantially all of the external surfaces of the electronic package, *with the exception of a portion of the conductors that are required for electrically coupling to an external substrate*, with an essentially hermetic covering which is highly hydrophobic," and that "the reduced level of moisture improves product yields and reliability thru the final assembly and testing processes." Havens et al., Page 2, Paragraph [0025] (emphasis added). Whether the carrier bonds are attached to the conductive leads of the device before or after applying the hermetic covering, substantially all of the external surfaces of the electronic package are covered by the hermetic covering, with the exception of a portion of the conductors that are required for electrically coupling to an external substrate. Therefore, Havens et al. clearly teaches that the hermetic covering improves reliability and product yield regardless of whether the carrier bonds are attached before or after applying the hermetic covering.

The Office also notes at Pages 6-7 of the outstanding Office Action that Havens et al. states "[i]n one embodiment, all of the package, including all of the external conductor surfaces, are covered (e.g., to facilitate shipment)," and appears to assert that this statement teaches or suggests that attaching the carrier bonds to the conductive leads of the device taught therein before applying the hermetic covering of Havens et al. to the structure of King et al. would "facilitate shipment" of the resulting structure. Appellants respectfully disagree. Havens et al. provides no indication whatsoever as to how shipment is facilitated by covering all external surfaces of the package with the hermetic covering. There is simply no description, teaching, or suggestion in Havens et al. as to how shipment of a package in which all of the external conductor surfaces are covered with the hermetic covering is improved, enhanced, or otherwise facilitated relative to shipment of a package in which substantially all of the external surfaces of the electronic package are covered with the hermetic covering, with the exception of a portion of the conductors that are required for electrically coupling to an external substrate, as in embodiments in which the carrier bonds are attached after applying the hermetic covering. In fact, Havens et al. expressly teaches that an electronic package having a "hydrophobic protective covering over substantially all of the external surfaces of the package, except for those portions of conductors that were covered by the cover layer," is "ready for shipment." Havens et al., Page 4, Paragraph [0047].

Furthermore, Appellants respectfully assert that one of ordinary skill in the art would recognize that, in methods in which the carrier bonds are attached after applying the hermetic covering, the electronic package could be shipped prior to attaching the carrier bonds, in which

case all of the package, including all of the external surfaces, would be covered by the hermetic covering.

In sum, there simply is no teaching or suggestion in the cited prior art references that any benefit would be achieved by attaching the carrier bonds to the conductive leads of the device taught by King et al. prior to applying the hermetic covering taught by Havens et al. In other words, the prior art references do not teach or suggest the desirability of attaching the carrier bonds to the conductive leads in the device taught by King et al. before applying the hermetic covering of Havens et al. instead of after applying the hermetic covering. In contrast, however, attaching the carrier bonds to the conductive leads of the device taught by King et al. after applying the hermetic covering taught by Havens et al. accords with the teachings of both Havens et al. and King et al. and would require less modification of the teachings of King et al. Therefore, one of ordinary skill in the art, considering the teachings of King et al. and Havens et al. in combination and as a whole at the time the present invention was made, clearly would have been motivated to attach the carrier bonds to the leads of the device after applying the hermetic covering taught by Havens et al. to the device taught by King et al.

Appellants respectfully assert that the Office appears to be using improper hindsight and combining the cited prior art references solely on the basis of the Appellants disclosure in the present application.

As there is no suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to combine the teachings of Havens et al. with the teachings of King et al. in the manner proposed by the Office, Appellants

respectfully assert that the Office has failed to establish a *prima facie* case of obviousness with respect to each of independent Claims 1 and 2, and request that the Board overturn the rejection of independent Claims 1 and 2 under 35 U.S.C. § 103(a).

Furthermore, Appellants assert that the non-obviousness of independent Claim 2 precludes a rejection of Claims 5 through 9, 13, 15, 16, and 19, each of which depends from Claim 2, because a dependent claim is obvious only if the independent claim from which it depends is obvious. See, In re Fine, 5 U.S.P.Q.2d 1596, 1600 (Fed. Cir. 1988), see also MPEP § 2143.03. At least for this reason, Appellants request that the Board overturn the rejection of dependent Claims 5 through 9, 13, 15, 16, and 19 under 35 U.S.C. § 103(a).

(ii) Claim 14

Appellants submit that the obviousness rejection of Claim 14 is improper and should be reversed because the Office has failed to identify a sufficient motivation to combine the teachings of Havens et al. with the teachings of King et al. in the manner proposed by the Office, as previously discussed in Section (7)(A)(i) above.

Appellants also assert that the obviousness rejection of Claim 14 is improper and should be reversed for the additional reason that King et al. and Havens et al., when combined, do not teach or suggest all the limitations of Claim 14. In particular, Appellants assert that King et al. and Havens et al., when combined, do not teach or suggest "[a] plurality of conductive carrier bonds [comprising] a conductive or conductor-filled polymer," as recited in dependent Claim 14.

King et al. teaches that the external electrodes 28 (shown in Figures 1 through 5 and 8 thereof) may comprise solder balls (King et al., Column 2, Lines 23-26; Column 4, Lines 49-65), but does not teach or suggest that they may comprise a conductive or conductor-filled polymer. Similarly, Havens et al. teaches that the conductors 6 (shown in Figures 1, 1A, 1B, 2, 2A, 3, 3A, 4, 4A, 5, 6, 6A, and 7) thereof may comprise solder balls (Havens et al., Page 2, Paragraph [0028]; Page 3, Paragraph [0030]; Page 4, Paragraph [0046]; Page 5, Paragraphs [0056]-[0058]), but does not teach or suggest that they may comprise a conductive or conductor-filled polymer.

As there is no suggestion or motivation to combine the teachings of Havens et al. with the teachings of King et al. in the manner proposed by the Office, and because King et al. and Havens et al. do not teach or suggest all the limitations of Claim 14, Appellants respectfully assert that the Office has failed to establish a *prima facie* case of obviousness with respect to dependent Claim 14, and request that the Board overturn the rejection of dependent Claim 14 under 35 U.S.C. § 103(a).

(B) The Second Rejection

(i) Claims 3, 4, and 10-12

Each of Claims 3, 4, and 10 through 12 depends either directly or indirectly from independent Claim 2, and, as a result, each includes the limitations recited in independent Claim 2. Appellants assert that the U.S. Patent and Trademark Office (the "Office") has failed to establish a *prima facie* case of obviousness with respect to Claims 3, 4, and 10 through 12

because the Office has failed to identify a sufficient motivation to combine the teachings of King et al. with the teachings of Havens et al. in the manner proposed by the Office.

As previously discussed in Section (7)(A)(i), King et al. and Havens et al., when combined, do not teach or suggest an intermediate structure as recited in independent Claim 2, from which each of Claims 3, 4, and 10 through 12 depends. The teachings of Lee et al. do not satisfy the deficiencies.

Lee et al. teaches providing a plurality of carrier bonds in the form of solder balls 16 on exposed upper surfaces of external connection means 34 *after* encapsulating a chip and lead frame assembly. Lee et al., Column 5, Lines 20-29, and 39-43; Figures 11-12. Therefore, Lee et al. also fails to provide any teaching or suggestion for forming external electrodes 28 on the conductive leads 12 of King et al. before providing a hermetic covering as taught by Havens et al. thereon in such a manner as to provide an intermediate structure as recited in independent Claim 2.

As there is no suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to combine the teachings of Havens et al. with the teachings of King et al. in the manner proposed by the Office, Appellants respectfully assert that the Office has failed to establish a *prima facie* case of obviousness with respect to each of dependent Claims 3, 4, and 10 through 12, and request that the Board overturn the rejection of these Claims under 35 U.S.C. § 103(a).

8) CLAIMS APPENDIX

A copy of Claims 1 though 16 and 19, as currently pending, is appended hereto in a "Claims Appendix."

9) EVIDENCE APPENDIX

The following documents are appended hereto as exhibits in an "Evidence Appendix:"

A copy of United States Patent No. 5,677,566 (King et al.) is appended hereto as "Evidence Exhibit 1."

A copy of United States Patent Application Publication No. 2001/0011773 A1 (Havens et al.) is appended hereto as "Evidence Exhibit 2."

A copy of United States Patent No. 5,894,107 (Lee et al.) is appended hereto as "Evidence Exhibit 3."

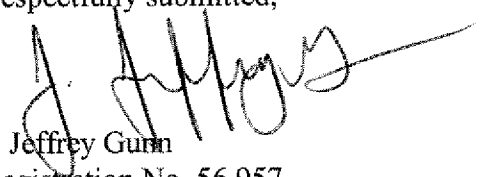
10) RELATED PROCEEDINGS APPENDIX

A copy of the Decision on Appeal mailed November 19, 2004 for Appeal No. 2004-2144, which was previously filed in prosecution of the present application, is attached hereto in a "Related Proceedings Appendix."

CONCLUSION

Appellants respectfully submit that Claims 1 through 16 and 19 are allowable over the cited references of record. Appellants respectfully request that the rejections of Claims 1 through 16 and 19 under 35 U.S.C. § 103(a) be reversed.

Respectfully submitted,



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CLAIMS APPENDIX

U.S. Patent Application No. 09/483,712

Filed January 14, 2000

Claims 1-16 and 19

1. An intermediate structure in the fabrication of a chip-scale package comprising:

a semiconductor die having an active surface having at least one bond pad thereon, sides and a back side;

at least one conductive lead frame member laterally spaced from the at least one bond pad and having an upper surface and a lower surface, the lower surface of the at least one conductive lead frame member having and inner end and an outer end and being substantially non-conductively attached to a portion of the active surface of the semiconductor die and vertically spaced therefrom by a non-coextensive dielectric element interposed therebetween;

at least one discrete conductive bond connecting the inner end of the at least one conductive lead frame member to the at least one bond pad on the active surface of the semiconductor die;

at least one carrier bond directly attached to the upper surface of the at least one conductive lead frame member at the outer end thereof and extending transversely thereto; and

wherein the intermediate structure is free of an encapsulant material to be subsequently applied to the intermediate structure.

2. An intermediate structure in the fabrication of a chip-scale package comprising:

a semiconductor die having an active surface having a plurality of bond pads thereon;

a dielectric element having an upper surface and a lower surface, the lower surface of the dielectric element attached to a portion of the active surface of the semiconductor die;

a plurality of conductive lead frame members having inner ends laterally spaced from the plurality of bond pads, each conductive lead frame member of the plurality of conductive lead frame members having an upper surface and a lower surface, a portion of the lower surface of each conductive lead frame member of the plurality of conductive lead frame members being attached to a portion of the upper surface of the dielectric element for connecting each conductive lead frame member of the plurality of conductive lead frame members to the active surface of the semiconductor die;

a plurality of discrete conductive bond members, at least one discrete conductive bond member of the plurality of conductive bond members connecting the inner end of each conductive lead frame member of the plurality of conductive lead frame members to at least one bond pad of the plurality of bond pads on the active surface of the semiconductor die;

a plurality of conductive carrier bonds, at least one carrier bond of the plurality of conductive carrier bonds directly disposed on the upper surface of each conductive lead frame member of the plurality of conductive lead frame members at a location remote from the inner end thereof and extending transversely from the upper surface thereof; and

wherein the intermediate structure is free of an encapsulant material to be subsequently applied to the intermediate structure.

3. An intermediate structure as in claim 2, wherein the dielectric element includes an adhesive-coated polyimide tape.

4. An intermediate structure as in claim 2, wherein the dielectric element includes a polyimide film.

5. An intermediate structure as in claim 2, wherein the upper surface and lower surface of the dielectric element are attached respectively to a portion of the lower surface of each conductive lead frame member of the plurality of conductive lead frame members and a portion of the active surface of the semiconductor die connecting portions of the plurality of conductive lead frame members to portions of the active surface of the semiconductor die.

6. An intermediate structure as in claim 2, wherein the plurality of conductive lead frame members comprises a plurality of lead fingers.

7. An intermediate structure as in claim 2, wherein the plurality of conductive lead frame members comprises a conductive metal.

8. An intermediate structure as in claim 2, wherein the plurality of discrete conductive bond members comprises a conductive metal.

9. An intermediate structure as in claim 2, wherein the plurality of discrete conductive bond members comprises bond wires.

10. An intermediate structure as in claim 9, wherein the bond wires comprise gold or aluminum.

11. An intermediate structure as in claim 2, wherein the plurality of discrete conductive bond members comprises TAB bonds.

12. An intermediate structure as in claim 2, wherein the plurality of discrete conductive bond members comprises thermocompression bonds.

13. An intermediate structure as in claim 2, wherein the plurality of conductive carrier bonds includes metal.

14. An intermediate structure as in claim 2, wherein the plurality of conductive carrier bonds comprises a conductive or conductor-filled polymer.

15. An intermediate structure as in claim 2, wherein the plurality of conductive carrier bonds is selectively located on the upper surfaces of the plurality of conductive lead frame members, forming an array over the active surface of the semiconductor die.

16. An intermediate structure as in claim 2, wherein the plurality of conductive carrier bonds comprises solder balls.

19. An intermediate structure as in claim 2, wherein each conductive carrier bond of the plurality of conductive carrier bonds further comprises an upper portion and a lower portion, the lower portion of each conductive carrier bond being attached to the upper surface of an associated conductive lead frame member of the plurality of conductive lead frame members.

EVIDENCE APPENDIX

U.S. Patent Application No. 09/483,712

Filed January 14, 2000

Evidence Exhibit 1 - United States Patent No. 5,677,566

Evidence Exhibit 2 - United States Patent Application Publication No. 2001/0011773 A1

Evidence Exhibit 3 - United States Patent No. 5,894,107

US005677566A

United States Patent [19]

King et al.

[11] Patent Number: 5,677,566

[45] Date of Patent: Oct. 14, 1997

[54] SEMICONDUCTOR CHIP PACKAGE

[75] Inventors: **Jerrold L. King**, Boise; **Jerry M. Brooks**, Caldwell, both of Id.

[73] Assignee: **Micron Technology, Inc.**, Boise, Id.

[21] Appl. No.: **436,522**

[22] Filed: **May 8, 1995**

[51] **Int. Cl.**[6] **H01L 23/495**

[52] **U.S. Cl.** **257/666**; 257/692; 257/738; 257/778; 257/787

[58] **Field of Search** 257/666, 778, 257/787, 692, 738

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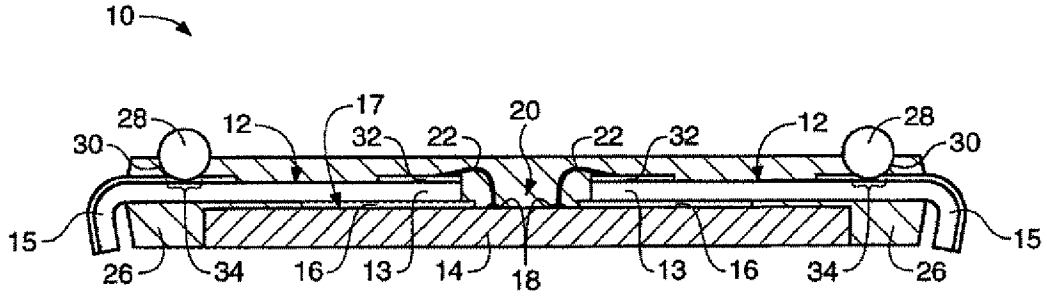
Attorney, Agent, or Firm—Ormiston Korfanta Dunbar & Holland, PLLC

[57] **ABSTRACT**

A semiconductor chip package that includes discrete conductive leads in electrical contact with bond pads on a semiconductor chip. This chip/lead assembly is encapsulated within an encapsulating material and electrode bumps are formed through the encapsulating material to contact the conductive leads. The electrode bumps protrude from the encapsulating material for connection to an external circuit.

18 Claims, 3 Drawing Sheets



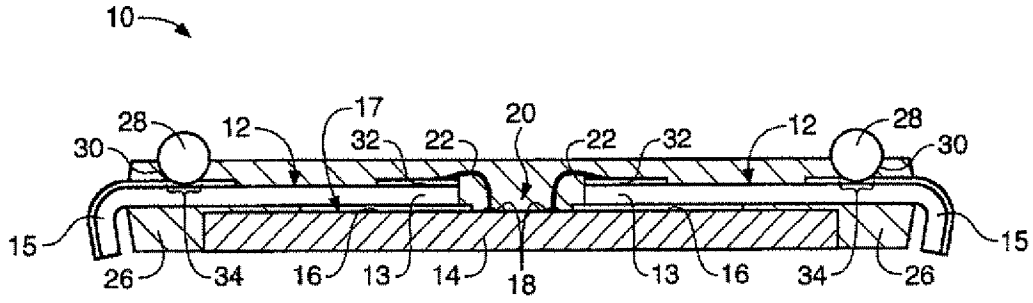


FIG. 1

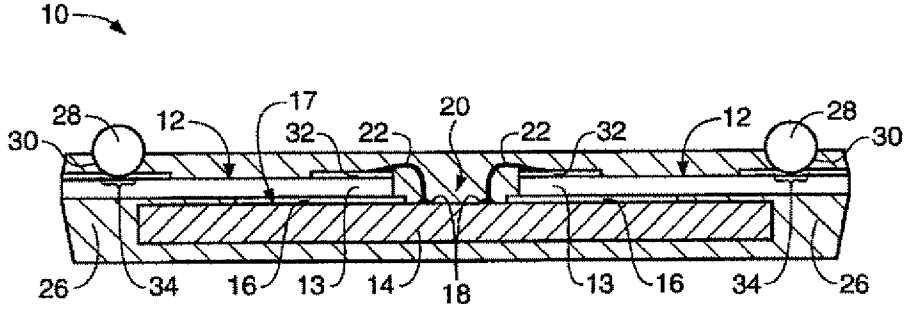


FIG. 2

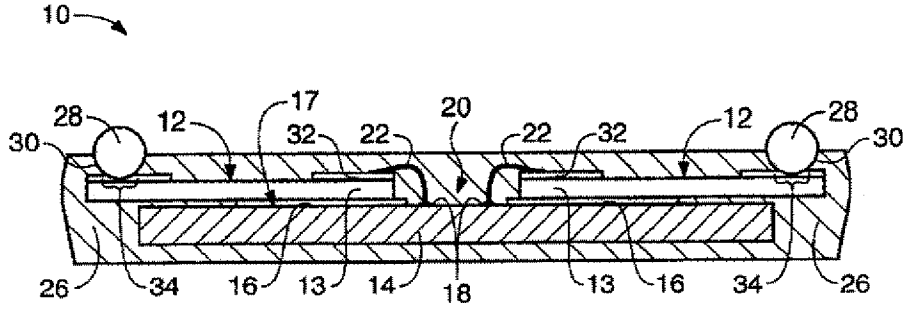


FIG. 3

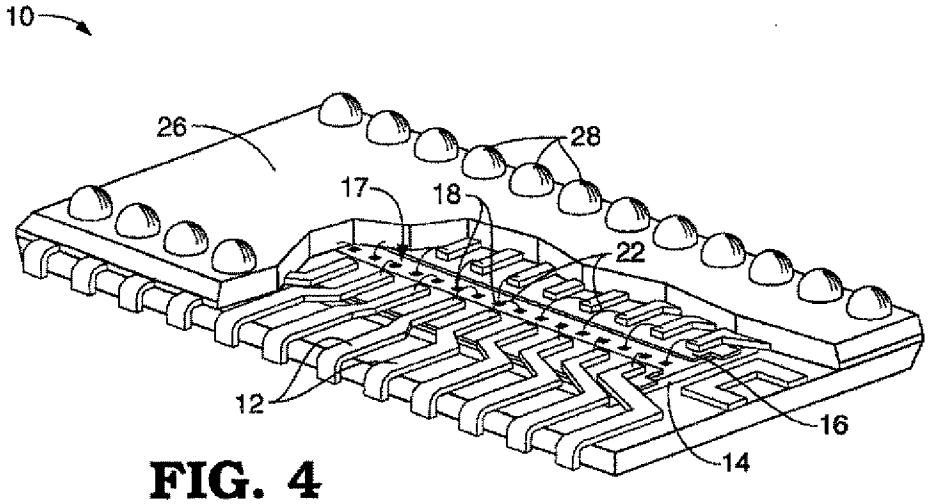
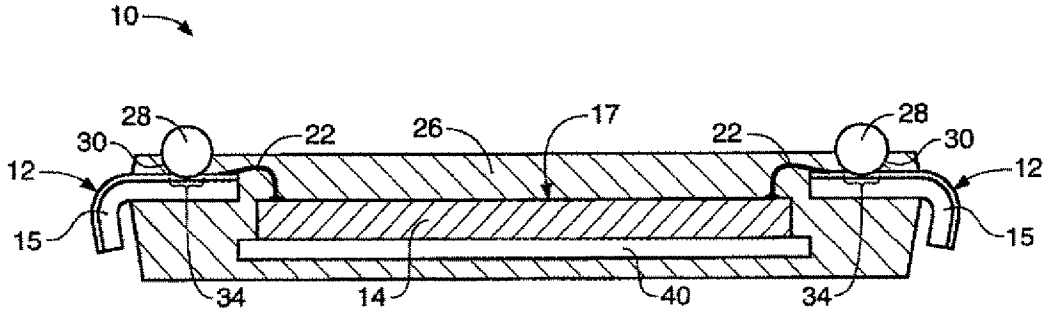

10
26
28
17
18
22
12
16
14

FIG. 4


10
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26
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FIG. 5

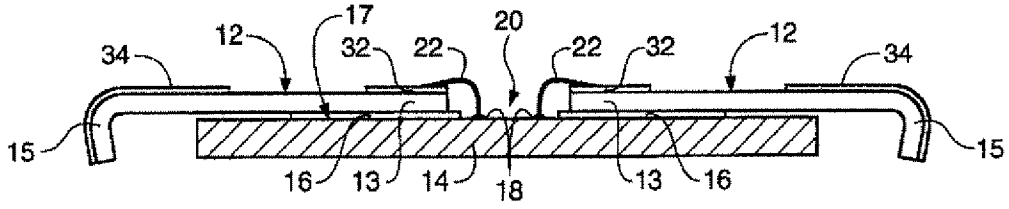

FIG. 6

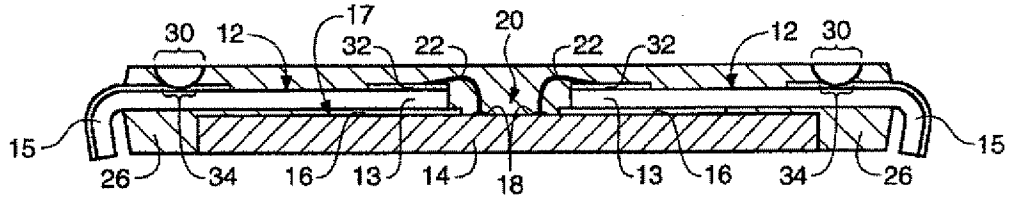

FIG. 7

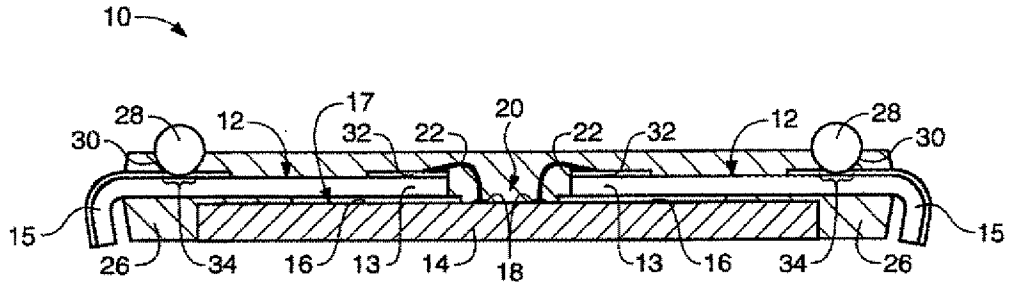

FIG. 8

SEMICONDUCTOR CHIP PACKAGE

FIELD OF THE INVENTION

This invention relates generally to semiconductor chip packages and, more particularly, to a molded semiconductor chip package having external electrode bumps connected to discrete conductive leads that are in electrical contact with the bond pads on the chip.

BACKGROUND OF THE INVENTION

In response to the demand for semiconductor chip packages having high lead counts and small footprints, ball grid array (BGA), "flip chip" and, more recently, "chip scale" packages have been developed. These packages are surface mounted to an external printed circuit board using an array of solder balls or similar electrode bumps, instead of metal leads. A BGA package utilizes a printed circuit board type substrate instead of a lead frame. In a typical BGA package, the semiconductor chip is mounted to the top surface of a substrate. The chip is wire bonded to electrical traces in the substrate. The chip is then overmolded with an encapsulating material. Solder balls are bonded to the electrical traces in the bottom surface of the substrate. The solder balls serve as the external electrodes for surface mounting on a printed circuit board.

Flip chip packages are similar to BGA packages, except that the solder balls are attached directly to the bond pads or electrical traces formed in the surface of the chip resulting in a more compact package. Due to the absence of an encapsulating material, flip chip packages are quite fragile and require careful assembly and handling techniques. Chip scale packages are being developed to combine the durability of the BGA packages and the small size of the flip chip packages. In a chip scale package, solder balls are attached to electrical traces in the surface of the chip or directly to the bond pads through openings in the encapsulating material. The electrical traces connect the solder balls, which form external electrode bumps, to the bond pads in the chip. The chip scale package need only be slightly larger then the bare chip because the electrode bumps are formed on the surface of the chip.

It is desirable that the new smaller semiconductor chip packages be adapted for use in standard formats developed for larger chips. However, for both the flip chip and chip scale packages, in which the electrode bumps are attached directly to contacts on the surface of the chip, the electrode bump array must be reconfigured each time the chip is made smaller. Hence, the corresponding contacts on the printed circuit board to which the package is ultimately assembled (the chip "footprint"), must also be reconfigured. In addition, there remains a need for a semiconductor chip package that combines the small size of chip scale packages with the durability and economies of conventional lead frame assemblies and encapsulating techniques currently used to form molded plastic packages.

SUMMARY OF THE INVENTION

It is one object of the present invention to combine the small size of chip scale type packages with the durability and economies of conventional lead frame assemblies and encapsulating techniques.

It is another object of the invention to utilize an array of bump electrodes configured independent of the size of the semiconductor chip so that the package is compatible for use with standard formats developed for larger chips.

These and other objects and advantages are achieved by a semiconductor chip package that includes discrete conductive leads in electrical contact with bond pads on a semiconductor chip. This chip assembly is encapsulated within an encapsulating material such as a thermosetting epoxy resin. Electrode bumps are formed through openings in the encapsulating material to contact the conductive leads. The electrode bumps protrude from the encapsulating material for connection to an external circuit.

In one preferred embodiment of the invention, the package comprises a semiconductor chip having bond pads disposed thereon, the bond pads being accessible from an upper surface of the chip. Conductive leads, which extend over and are attached to the upper surface of the chip, are electrically connected to the bond pads. An encapsulating material covers at least a portion of the upper surface of the chip, the bond pads, and the leads. If desired, the entire assembly may be fully encapsulated. Alternatively, the conductive leads may extend out from the encapsulating material. Openings are formed in the encapsulating material to expose portions of the leads. Electrodes are formed through the openings in the encapsulating material and bonded to the exposed portions of the leads. These electrodes, typically solder balls, can then be surface mounted to a printed circuit board in the same way BGA and chip scale packages are mounted.

The conductive leads may be part of a conventional lead frame and the assembly encapsulated using equipment and techniques currently used to form molded plastic packages. The ends of the leads may extend out of the encapsulating material with or without forming to facilitate testing and burn-in. After testing, the leads may be severed flush with the encapsulating material or left extending from the package. Alternatively, the leads may be severed prior to encapsulation and the assembly fully encapsulated.

As noted, the semiconductor chip package of the present invention can be assembled using conventional molded plastic packaging techniques, equipment and materials. Further, because the electrode bumps are not connected directly to the bond pads or electrical traces in the semiconductor chip, the size of the package and the configuration of the electrode bump array can remain the same even as the chip is made smaller, thus allowing the package to be constructed to a standard format.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a cross section view of one embodiment of the invention wherein the encapsulating material covers the upper surface of the semiconductor chip and the conductive leads are positioned over the chip and extend outside the encapsulating material.

FIG. 2 is a cross section view of a second embodiment of the invention wherein the semiconductor chip is fully encapsulated and the conductive leads are positioned over the chip and severed flush with the edge of the encapsulating material.

FIG. 3 is a cross section view of a third embodiment of the invention wherein the semiconductor chip and conductive leads are fully encapsulated.

FIG. 4 is a perspective view of the embodiment of FIG. 1 wherein part of the encapsulating material has been cut away to show the upper surface of the semiconductor chip, the conductive leads and the solder balls.

FIG. 5 is a cross section view of a fourth embodiment of the invention wherein the conductive leads are positioned adjacent to the semiconductor chip.

FIGS. 6–8 are cross section views of the embodiment of FIG. 1 at various stages of fabrication.

The figures are not meant to be actual views of the various embodiments, but merely idealized representations used to depict the structure and manufacture of the invention.

DETAILED DESCRIPTION OF THE INVENTION

FIG. 1 is a cross section view of a semiconductor chip package **10** constructed according to one of the preferred embodiments of the invention. FIG. 4 is a perspective view of the chip package of FIG. 1 wherein part of the encapsulating material has been removed. Referring to FIGS. 1 and 4, conductive leads **12**, which comprise the inner portion of a conventional lead frame (not shown), are attached to a semiconductor chip **14** by a layer of adhesive material **16**. Bond pads **18** are aligned along the central portion **20** of semiconductor chip **14**. Bond pads **18** represent any of the various terminals commonly formed near the surface of a semiconductor chip through which electrical connections are made between active devices in the chip and external circuits.

The configuration of the chip package illustrated in FIGS. 1 and 4 is commonly referred to as a "lead over chip" (LOC) package because the conductive leads **12** extend over the semiconductor chip **14** and are bonded to the centrally located bond pads **18**. Bond wires **22** connect conductive leads **12** to bond pads **18**. The semiconductor chip assembly, which includes chip **14**, bond pads **18** and inner end **13** of conductive leads **12**, is encapsulated within an encapsulating material **26**. External electrodes **28** are connected to conductive leads **12** through openings **30** formed in encapsulating material **26**. External electrodes **28** may be positioned at desired locations along conductive leads **12**. The conductive leads **12** are typically plated with a thin layer of metal suitable for wire bonding, such as gold, silver or palladium/nickel, at wire bond area **32** to improve the strength and conductivity of the bond between conductive leads **12** and bond wires **22**. Similarly, conductive leads **12** may be plated with a thin layer of metal suitable for the solder connection, usually gold, palladium/nickel, or tin, at electrode bond area **34** to improve the strength and conductivity of the bond between conductive leads **12** and external electrodes **28**. In this embodiment, the outer end **15** of conductive leads **12** extends out from the encapsulating material to facilitate chip testing using equipment and techniques presently used to test conventional external lead plastic packages. The external leads may be sheared after testing to provide a more compact package as shown in FIG. 2.

In an alternative embodiment of the invention, shown in FIG. 2, the semiconductor chip **14** is fully encapsulated and the conductive leads sheared flush with the encapsulated material. This embodiment utilizes the same components as the preferred embodiment and results in a stronger but thicker package. In a third embodiment, illustrated in FIG. 3, the ends of the conductive leads **12** that would otherwise extend outside the encapsulating material are sheared prior to encapsulation so that the entire assembly is encapsulated.

The invention may also be incorporated into a chip package wherein the bond pads are located along the periphery of the chip and wire bonded to adjacent leads. Referring to FIG. 5, semiconductor chip **14** is mounted on leadframe die paddle **40**. Conductive leads **12** are wire bonded to bond pads **18** which are located along the periphery of chip **14**. External electrodes **28** are connected to conductive leads **12** through openings **30** formed in encapsulating material **26**.

The semiconductor chip package of the present invention can be formed using conventional molded plastic package lead frame assemblies and packaging processes and equipment. The invention is also advantageous over BGA and chip scale type packages because the electrode array can be configured and the package sized independent of the size of the semiconductor chip. The electrodes are connected to the conductive leads, not directly to the bond pads or wiring traces in the semiconductor chip as in known packages. Thus, the configuration of the electrodes as well as the size of the package can remain unchanged even as the chip size is reduced. Overall package dimensions can be controlled independent of chip size as necessary to accommodate standardized user requirements. Packaging equipment and processes need not be modified each time a reduction in chip size is achieved.

The fabrication of the package illustrated in FIGS. 1 and 4 will now be described with reference to FIGS. 6–8. Referring to FIG. 6, semiconductor chip **14**, which can be any integrated circuit device, is attached to conductive leads **12**. The active devices (not shown) within the chip are connected to centrally located bond pads **18**. Generally, bond pads **18** are exposed through apertures in an insulating or passivation layer which forms the top surface of the chip. Conductive leads **12**, which comprise the inner portion of a conventional lead frame (not shown), are positioned over the chip and extend to near the bond pads **18**. Conductive leads **12** are attached the upper surface **17** of chip **14** by an adhesive layer **16** using conventional processes known in the art. For example, one known process for attaching a semiconductor chip to LOC leads is disclosed in U.S. Pat. No. 5,286,679, issued to Farnworth et al. on Feb. 15, 1994, incorporated herein by reference. Conductive leads **12** are usually prefabricated with plating of a thin layer of suitable metal at wire and electrode bond areas **32** and **34**. Alternatively, conductive leads **12** may be plated after encapsulation and deflash (discussed below). Bond wires **22** are bonded to the bond pads **18** and the wire bond area **32** of the conductive leads **12** in a conventional manner well known in the art.

Referring to FIG. 7, the assembly is encapsulated within an encapsulating material **26**, typically a thermosetting epoxy resin, in a conventional manner. The encapsulating material **26** is formed with openings **30** to expose conductive leads **12** at electrode bond area **34**. Openings **30** are sized and shaped according to the size and shape of solder balls **38**, which form the external electrodes. Openings **30** are shown hemispherically shaped to correspond to a spherical solder ball. It is to be understood, however, that openings **30** could be any size and shape that corresponds to the desired size and shape of the external electrode. Any resin residue that is present on the electrode bond area after encapsulation is removed by electrolytic or mechanical deflash processes well known in the art.

Referring to FIG. 8, solder balls **38** are bonded to electrode bond area **34** of conductive leads **12**, which are exposed through openings **30**. The solder balls may be attached, as is known in the art, by coating the solder balls or bond areas with flux, placing the balls on the electrode bond area **34** through opening **30** with conventional pick and place or shaker/hopper equipment, and reflowing the balls in place using an infrared or hot air reflow process. The excess flux is then removed with an appropriate cleaning agent. In this way, the solder balls are electrically and mechanically connected to the conductive leads to form the external electrodes. Other processes may also be used to form the external electrodes. For example, the electrodes may be "plated up" using conventional plating techniques rather than formed using solder balls as described above. The completed semiconductor chip package can then be assembled to a printed circuit board or the like using conventional surface mount processes and equipment.

There has been shown and described a novel semiconductor chip package that can be made only slightly larger

than the chip using conventional leaded chip packaging processes and equipment and in which the array of bump electrodes can be sized and configured independent of the size of the chip. The particular embodiments shown in the drawings and described herein are for purposes of example and should not be construed to limit the invention as set forth in the appended claims. Those skilled in the art may now make numerous uses and modifications of the specific embodiments described without departing from the scope of the invention. The process steps described may in some instances be performed in a different order and/or equivalent structures and processes may be substituted for the various structures and processes described.

We claim:

1. A semiconductor chip package, comprising:

a. a semiconductor chip;

b. conductive leads electrically connected to the chip, the conductive leads extending over an upper surface of the chip;

c. encapsulating material covering at least a portion of the chip and at least a portion of the conductive leads, the encapsulating material having openings therein to expose electrode bond areas on the conductive leads; and

d. electrodes contacting the electrode bond areas through the openings in the encapsulating material.

2. A semiconductor chip package according to claim 1, wherein the bond pads are electrically connected to active devices formed in the chip.

3. A semiconductor chip package according to claim 1, wherein the encapsulating material encapsulates the chip and the conductive leads extend out through the encapsulating material.

4. A semiconductor chip package according to claim 1, wherein the electrodes comprise a plurality of solder balls each approximating the size and shape of the openings in the encapsulating material, the solder balls being bonded to the leads through the openings in the encapsulating material.

5. A semiconductor chip package, comprising:

a. a semiconductor chip;

b. conductive leads electrically connected to the chip;

c. encapsulating material encapsulating the chip and the conductive leads, the encapsuating material having openings therein to expose electrode bond areas on the conductive leads; and

d. electrodes contacting the electrode bond areas through the openings in the encapsulating material.

6. A semiconductor chip package, comprising:

a. a semiconductor chip having bond pads thereon, the bond pads being accessible from an upper surface of the chip;

b. conductive leads extending over and attached to the upper surface of the chip;

c. connecting means for electrically connecting the conductive leads to the bond pads;

d. encapsulating material covering at least a portion of the upper surface of the chip, the bond pads, at least a portion of the conductive leads and the connecting means, the encapsulating material having openings therein to expose electrode bond areas on the conductive leads; and

e. electrodes contacting the electrode bond areas through the openings in the encapsulating material.

7. A semiconductor chip package according to claim 6, wherein the bond pads are electrically connected to active devices formed in the chip.

8. A semiconductor chip package according to claim 6, wherein the bond pads are aligned along a central portion of the chip.

9. A semiconductor chip package according to claim 6, wherein the conductive leads are attached to the upper surface of the chip by a layer of adhesive material interposed between the conductive leads and the upper surface of the chip.

10. A semiconductor chip package according to claim 6, wherein the connecting means comprises a plurality of bond wires bonded to the conductive leads and the bond pads thereby electrically connecting the conductive leads to the bond pads.

11. A semiconductor chip package according to claim 6, wherein the encapsulating material is a thermosetting epoxy resin.

12. A semiconductor chip package according to claim 6, wherein the encapsulating material encapsulates the chip and the conductive leads extend out through the encapsulating material.

13. A semiconductor chip package according to claim 6, wherein the encapsulating material encapsulates the chip, the bond pads, the connection means and the conductive leads.

14. A semiconductor chip package, comprising:

a. a semiconductor chip assembly comprising a semiconductor chip and discrete conductive leads at spaced apart locations above and adjacent to and in electrical contact with the chip, the semiconductor chip assembly being disposed within an encapsulating material; and

b. electrode bumps extending through the encapsulating material to contact the conductive leads and protruding from the encapsulating material for connection to an external circuit.

15. A semiconductor chip package according to claim 14, wherein the conductive leads have an outer end that extends out from the encapsulating material.

16. A semiconductor chip package, comprising:

a. a semiconductor chip having active devices therein;

b. a plurality of bond pads electrically connected to the active devices, the bond pads being aligned along a central portion of one surface of the chip;

c. an insulating layer overlying the surface of the chip, the insulating layer having holes therein to enable electrical connection to the bond pads through the holes;

d. a plurality of discrete conducting leads extending over and attached to the insulating layer, each lead having an inner end and an outer end, the inner end being located in close proximity to the bond pads;

e. a plurality of bond wires bonded to wiring bond areas on the inner end of the leads and the bond pads on the chip thereby electrically connecting the leads to the bond pads;

f. an encapsulating material disposed over and enclosing the chip, the bond pads, the inner end of the conducting leads and the bond wires, the encapsulating material having openings formed therein to expose electrode bond areas on the inner end of the conductive leads; and

g. a plurality of solder balls each approximating the size and shape of the openings in the encapsulating material, the solder balls being bonded to the electrode bond areas through the openings in the encapsulating material.

17. A semiconductor chip package according to claim 16, wherein the size and shape of the openings is defined by a desired size and shape of the solder balls after a reflow step.

18. A semiconductor chip package according to claim 16, wherein the conductive leads are severed substantially flush with the encapsulating material after encapsulation.

* * * * *

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(12) **Patent Application Publication** (10) **Pub. No.: US 2001/0011773 A1**

HAVENS et al. (43) **Pub. Date: Aug. 9, 2001**

(54) **ELECTRONIC PACKAGE UTILIZING PROTECTIVE COATING**

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(21) Appl. No.: **09/276,596**

(22) Filed: **Mar. 25, 1999**

Related U.S. Application Data

(62) Division of application No. 08/939,302, filed on Sep. 29, 1997, now Pat. No. 5,888,850.

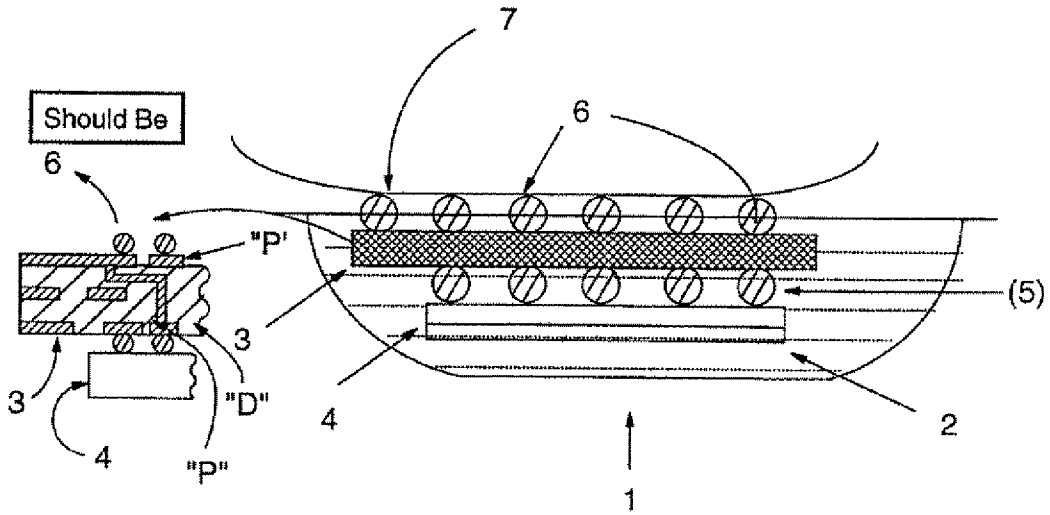
Publication Classification

(51) **Int. Cl.**[7] **H01L 23/48**; H01L 23/52; H01L 23/053; H01L 23/12; H01L 29/40; H01L 23/28; H01L 23/29

(52) **U.S. Cl.** **257/734**; 257/700; 257/701; 257/737; 257/738; 257/778; 257/781; 257/787; 257/788; 257/789

(57) **ABSTRACT**

The present invention is a method of providing a protective covering on an electronic package including a first circuitized substrate, a semiconductor chip positioned on and electrically coupled to the first substrate, and a plurality of conductors also on the substrate for electrically connecting the substrate to an external circuitized substrate. In one version, the method comprises covering substantially all of the external surfaces of the substrate, the semiconductor chip and a portion of the plurality of conductors with a protective covering from immersion in a dielectric solution (e.g., TEFLON AF). The coatings can also be applied by brushing, spraying, or chemical vapor deposition. In an alternative embodiment, all of the external surfaces, including all of the conductors, are coated with the protective covering (e.g., to facilitate package shipment or other handling). The resulting electronic packages are also described herein.



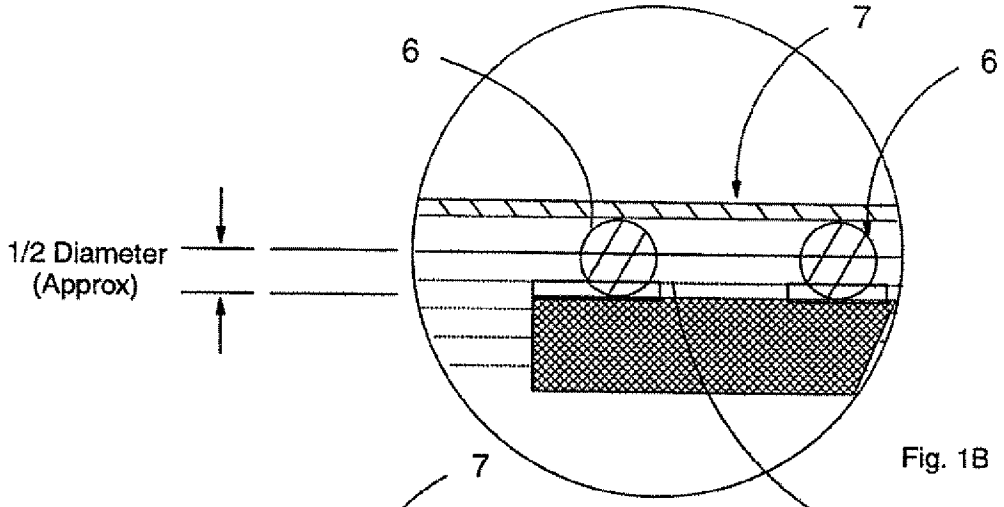


Fig. 1B

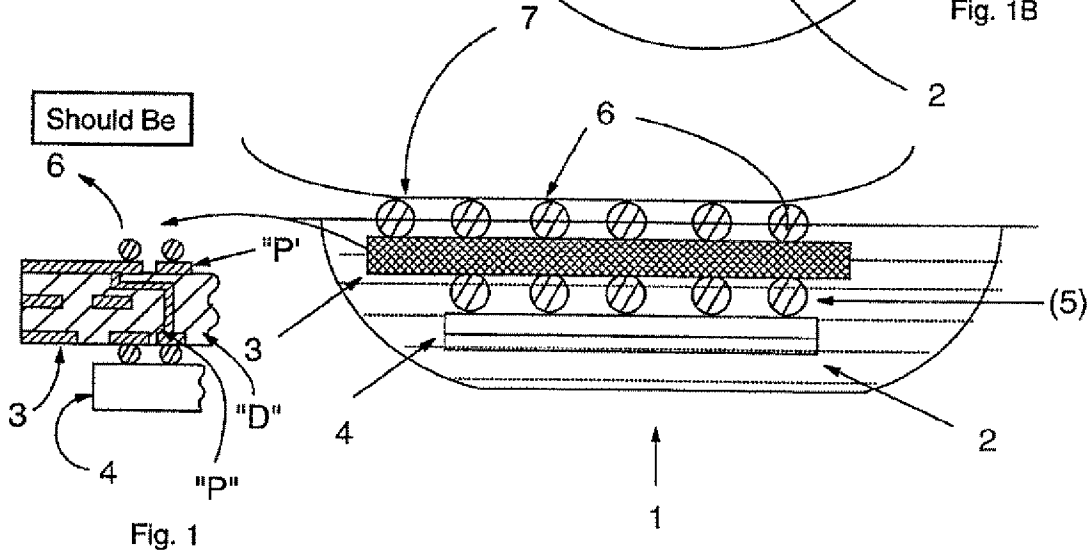


Fig. 1

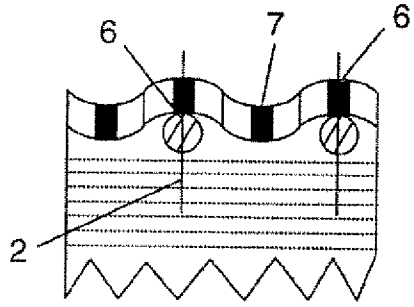


Fig. 1A

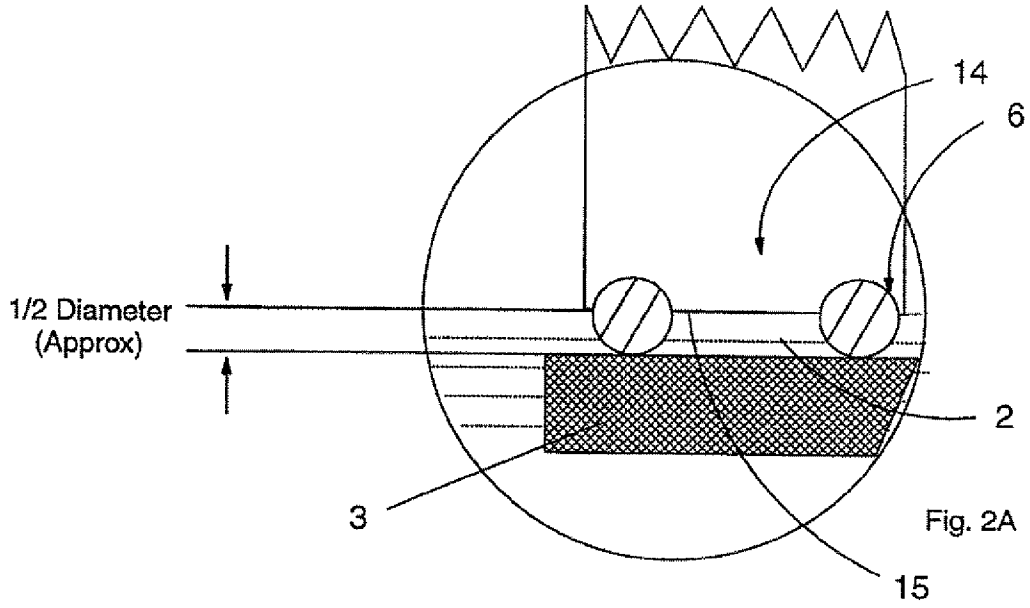


Fig. 2A

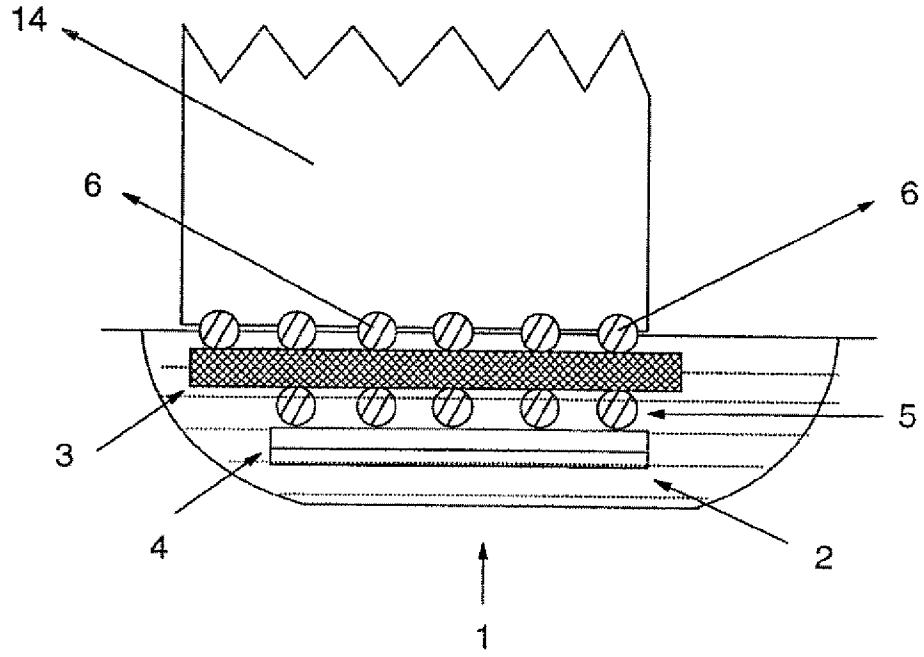


Fig. 2

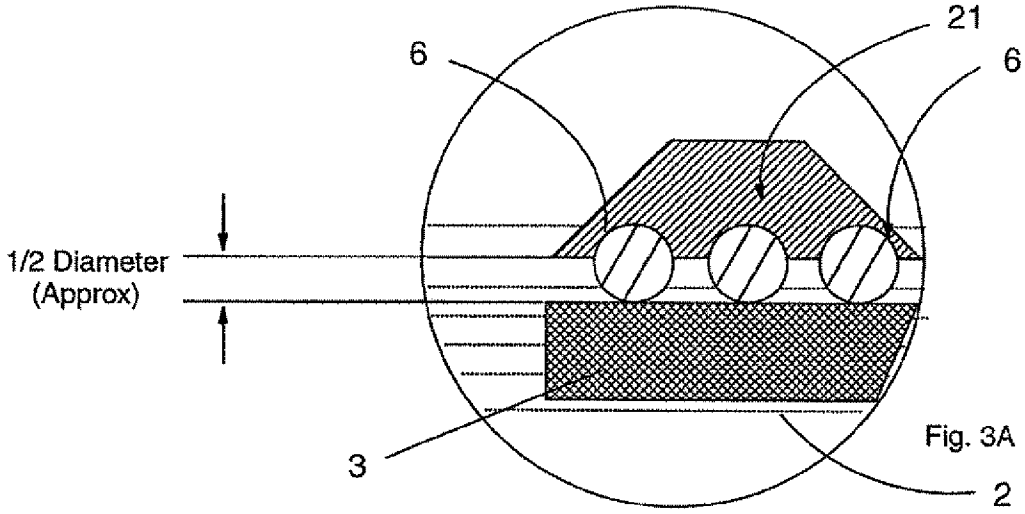


Fig. 3A

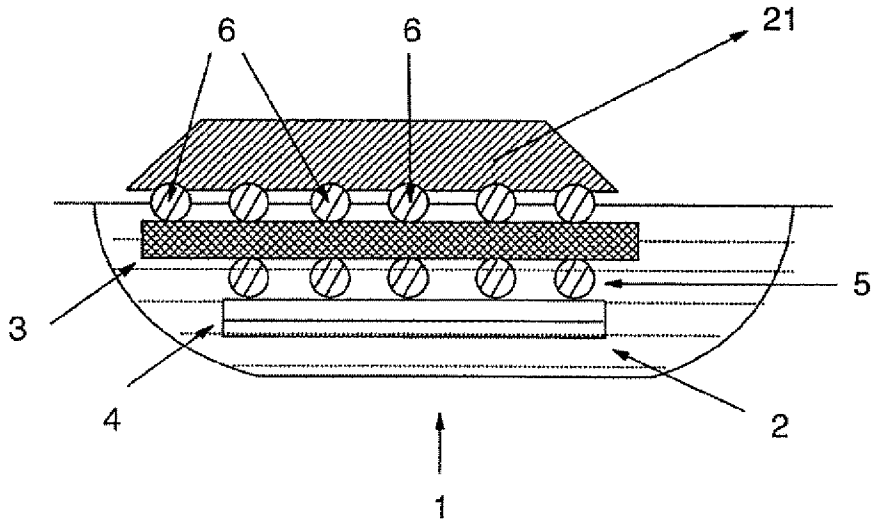


Fig. 3

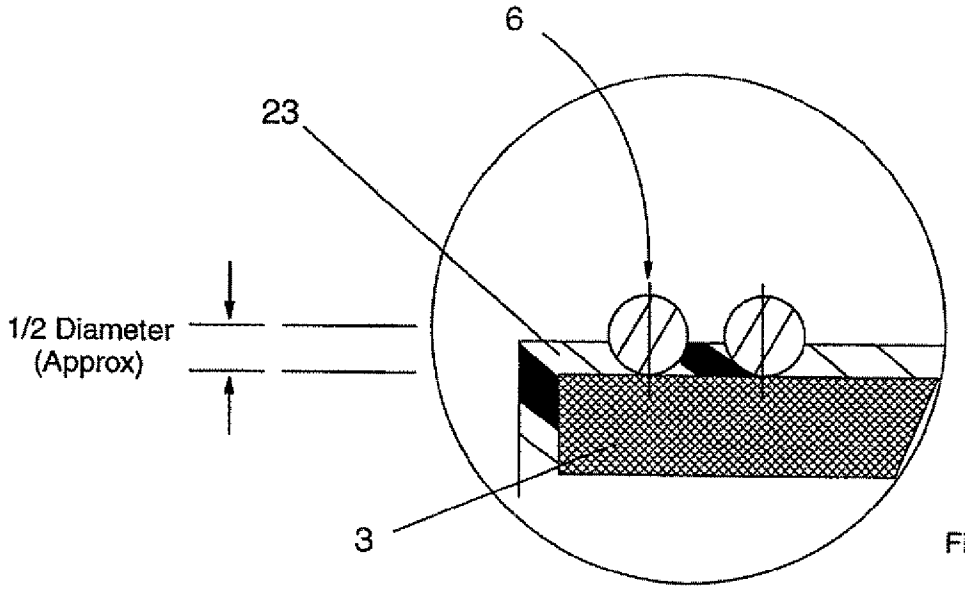


Fig. 4A

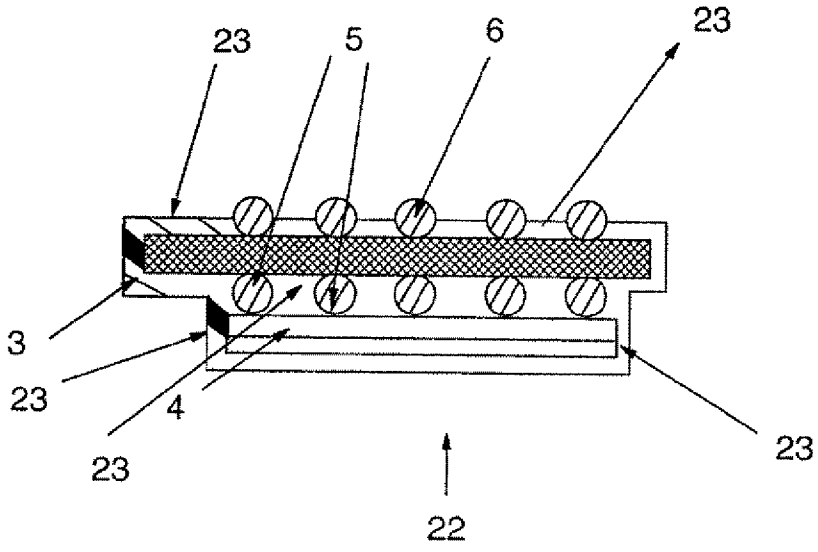


Fig. 4

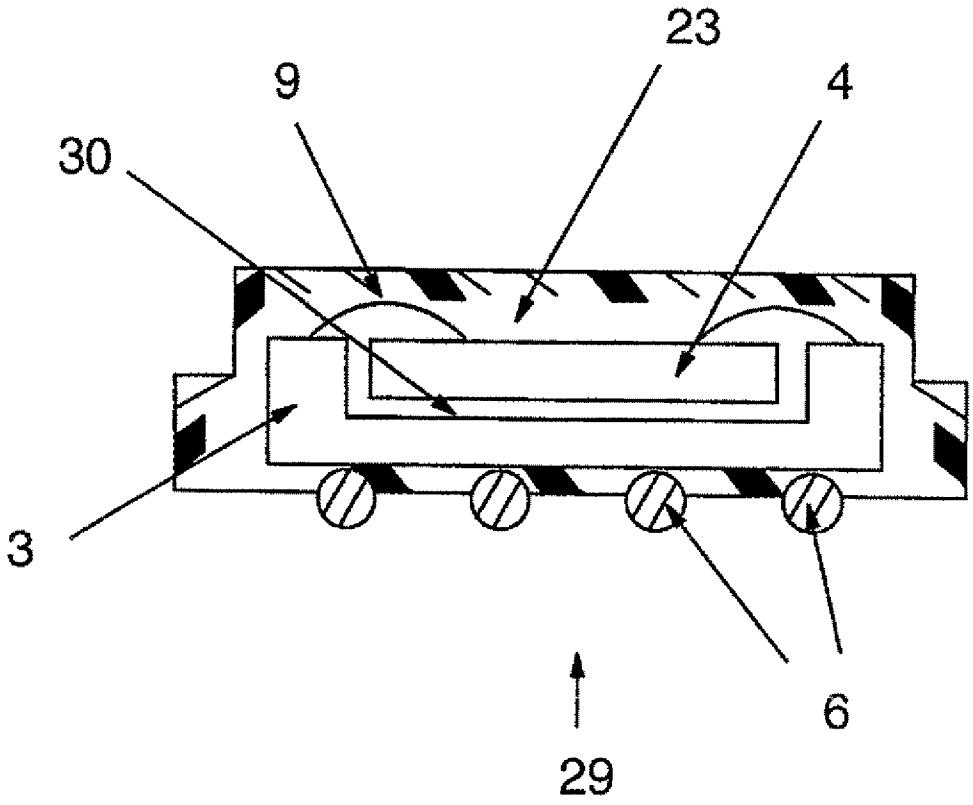


Fig. 5

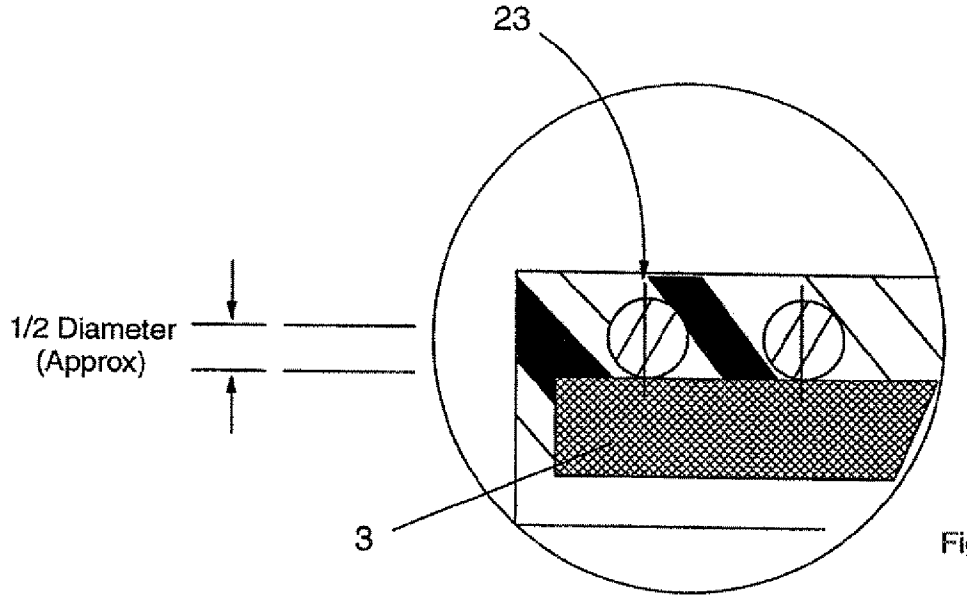


Fig. 6A

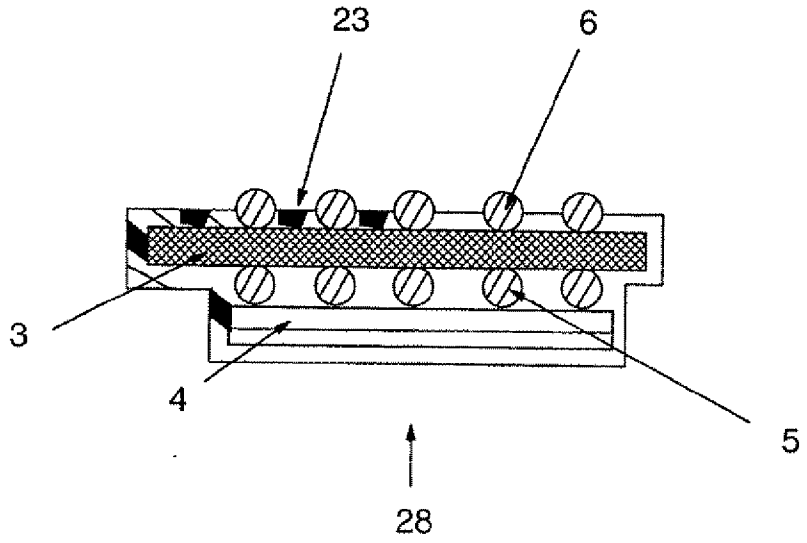


Fig. 6

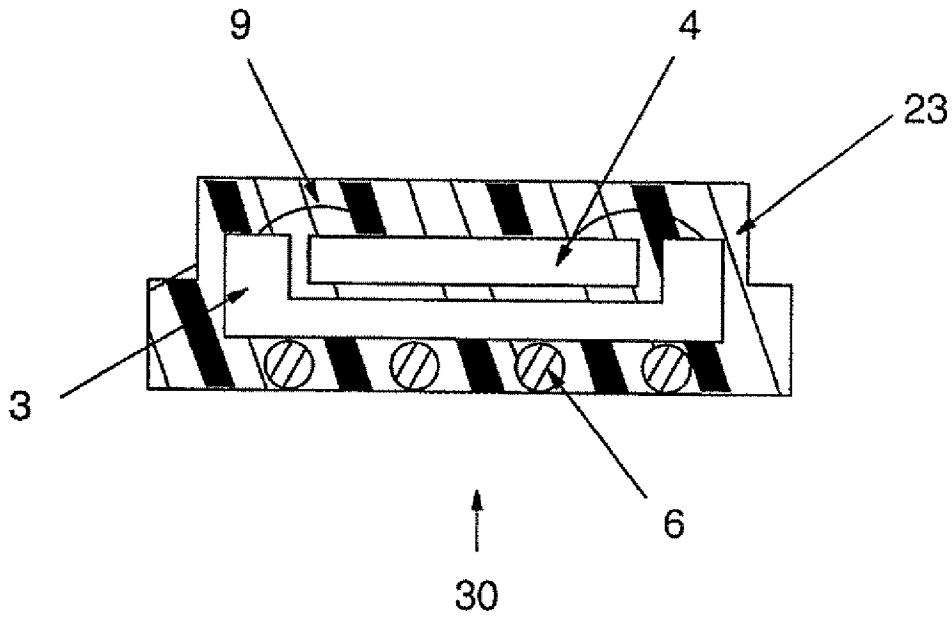


Fig. 7

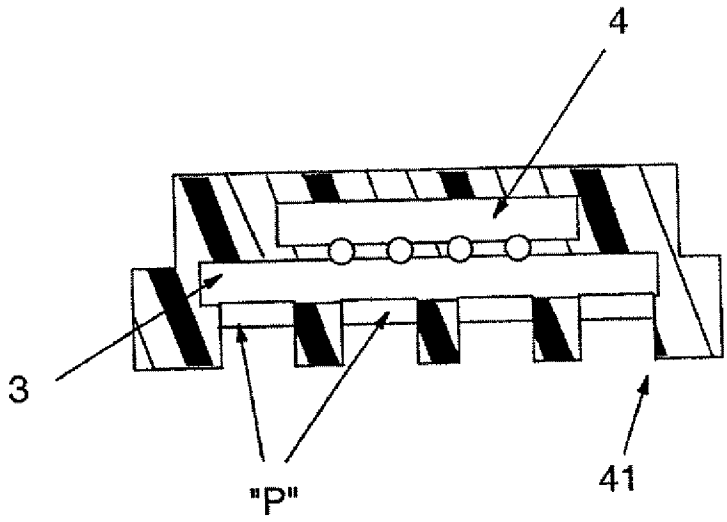


Fig. 9

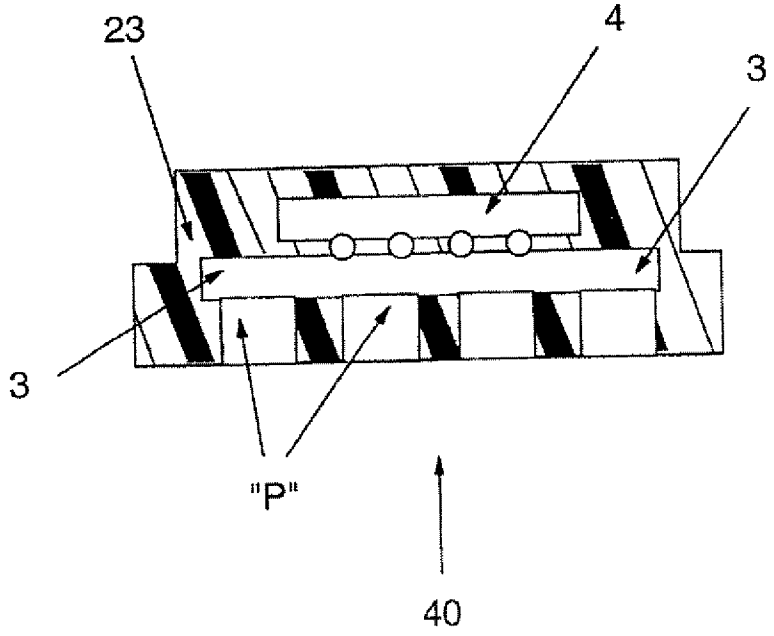


Fig. 8

ELECTRONIC PACKAGE UTILIZING PROTECTIVE COATING

FIELD OF THE INVENTION

[0001] This invention relates to a protective covering for an electronic package and, more particularly, to a dielectric protective covering for an electronic package comprising a semiconductor chip, a substrate, and conductors which may be used within an information handling system (computer).

BACKGROUND OF THE INVENTION

[0002] There have been previous attempts to apply coatings onto electronic packages, including attempts to encapsulate chips and conductors with the main emphasis of providing mechanical strength to the conductors. However, such efforts have not typically solved problems associated with moisture sensitivity.

[0003] In electronic chip carrier packages, moisture can cause various problems such as delamination, corrosion, formation of plated fiber shorts, chip cracking and debonding. This may result in yield loss and/or functional failure during assembly and reliability testing. Organic packages are particularly susceptible to moisture due to the hydrophilic nature of resins such as epoxies and polyimides when exposed to moisture, and are susceptible to the brittleness of glass reinforcement interfaces.

[0004] U.S. Pat. No. 5,474,957 to Urushima shows a process for building/assembling a chip onto a flexible film member. The assembly process involves using a piece of resin, to encapsulate the wire bond leads and act to hold the chip to the film. While the purpose of this resin is in part to prevent corrosion/oxidation, and to mechanically protect the wire bond leads, it is used in an entirely different location and with a completely different purpose than the present invention. U.S. Pat. No. 5,474,957 describes the use of a wire bond encapsulant which is applied only to the wire bond area. The present invention, on the other hand, involves using a protective coating over substantially the entire assembled package including, chip, wires (if used), or solder joints and the chip carrier.

[0005] U.S. Pat. No. 5,436,203 to Lin covers the concept of building an EMI shielded chip carrier package by shielding the chip and wire bonds. The bottom is shielded with a buried power plane or reference plane, and the top is shielded with a conductive encapsulate. The two shielding layers are electrically connected via plated thru holes. The chip and wire bonds are first covered with a non conductive encapsulant. Lin is different from the present invention for substantially the same reasons as Urushima above.

[0006] U.S. Pat. No. 5,496,775 to Brooks discloses using stacked and bonded metal balls as the electrical connection points. The chip is enclosed in an encapsulation material. The primary function of the encapsulant material appears to be to provide mechanical support for the chip and ball towers. The encapsulation is performed in two steps. First, a layer of encapsulant is formed within a mold or cavity. Next, the ball stacked chip is placed in the cavity and additional encapsulant is flooded into the mold and around the stacked ball towers. These two encapsulant layers form part of the chip package. The primary subject covered by Brooks appears to be the concept of using stacked metal balls as electrical leads, with the primary purpose of the encapsulant layer being to support and strengthen these leads.

[0007] U.S. Pat. No. 4,351,101 to Young shows a method of making connection to CCD (charged coupled device) chips. The method describes how metal pads are allowed to sink through a layer of uncured epoxy, via gravity, as an improvement over the previous method which involved hours of lapping (mechanical sanding).

[0008] U.S. Pat. No. 2,720,617 to Sardella covers a method of making a two-part case for early transistor packages, (circa 1955). The case consists of two pieces of TEFLON, (or other fluorocarbons), which are mechanically machined to form a hollow tube and a plug, both threaded. TEFLON is a trademark of E. I. du Pont de Nemours and Co., Inc. The transistor is placed into the tube, the tube is filled with epoxy encapsulant and the plug is screwed into the tube. The transistors are covered for improved resistance to vibration, moisture and mechanical damage.

[0009] The glasses used in electronic packaging of semiconductor and other electronic devices may successfully provide hermetic packaging; however, such glasses may create problems. Conventional sealing glasses are usually brittle and glass sealed semiconductor packages require special care in handling both during and subsequent to processing. This is necessary to avoid fracture of the glass and resulting loss of package hermeticity. The methods of applying the glass to the components to be sealed are also generally somewhat tedious and costly. One known method of applying the glass is to mix finely powdered glass with a suitable vehicle. The mixture is then silk screened in place upon the components. Next, the glass applied component is fired to coalesce the individual glass particles into a continuous glass coating in the areas previously silk screened. At the same time, any residue from the vehicle used during silk screening is driven off.

[0010] The present invention comprises a product (electronic package) and a method for making said product, that contains a semiconductor chip wherein substantially the entire electronic package is encapsulated with a solution which forms a protective coating sufficient to protect the electronic package from exposure to moisture and other adverse environmental conditions.

SUMMARY OF THE INVENTION

[0011] It is an object of the present invention to enhance the art of information handling systems. More particularly, it is an object of the present invention to provide an improved method for mass producing electronic packages. Further, it is an object of the present invention to provide an improved electronic package product.

[0012] In one aspect of the invention, there is provided a method of providing a protective covering on an electronic package including a substrate, a semiconductor chip positioned and electrically coupled to the substrate, and a plurality of conductors on the substrate for electrically connecting the substrate to an external substrate. The method comprises covering substantially all of the external surfaces of the substrate, the semiconductor chip and a portion of the plurality of conductors with a protective covering.

[0013] In accordance with another aspect of the invention, there is provided a method of providing a protective covering on an electronic package including a substrate, a semiconductor chip positioned on and electrically coupled to the substrate, and a plurality of conductors on the substrate for electrically coupling the substrate to an external substrate. In this aspect of the invention, substantially all of the external surfaces of the substrate, the semiconductor chip and the plurality of conductors are initially covered with the protective covering. Thereafter, a portion of the covering is removed from a portion of the external surfaces of the plurality of conductors.

[0014] According to another aspect of the invention, there is provided an electronic package comprising a first substrate, a semiconductor chip positioned on a first surface of the first substrate and electrically coupled to the substrate, a plurality of conductors located on a second surface of the first substrate for electrically coupling the first substrate to an external substrate, and a dielectric protective covering, substantially covering all of the external surfaces of the electronic package, except for a portion of the plurality of conductors.

[0015] According to yet another aspect of the invention, there is provided an electronic package comprising a substrate having first and second surfaces, a semiconductor chip positioned on the first surface of the substrate and electrically coupled to the substrate, a plurality of conductors located on the second surface of the substrate for electrically coupling the substrate to an external substrate, and a dielectric protective covering, substantially covering the entire external surfaces of the electronic package.

BRIEF DESCRIPTION OF THE DRAWINGS

[0016] **FIGS. 1, 1A**, and 1B show an immersion of an electronic package into a protective covering solution using tape as a suspending mechanism, according to one embodiment of the invention. **FIG. 1A** represents an alternative embodiment of the process wherein the tape acts both as a suspending mechanism and as a cover layer. **FIG. 1B** shows an enlarged view of a portion of **FIG. 1**.

[0017] **FIGS. 2 and 2A** show an immersion of an electronic package into a protective covering solution using a vacuum fixture on a portion of the conductors, according to another embodiment is of the invention. **FIG. 2A** shows an enlarged view of a portion of **FIG. 2**.

[0018] **FIGS. 3 and 3A** show an immersion of an electronic package into a protective covering solution using a cover layer on a portion of the conductors, according to another embodiment of the invention. **FIG. 3A** shows an enlarged view of a portion of **FIG. 3**.

[0019] **FIGS. 4 and 4A** show substantially all of an electronic package covered with a protective covering except for a portion of the conductors, according to another embodiment of the invention. **FIG. 4A** shows an enlarged view of a portion of **FIG. 4**.

[0020] **FIG. 5** shows substantially all of an electronic package covered with a protective covering except for a portion of the conductors. A semiconductor chip is wire bonded to the package's substrate.

[0021] **FIGS. 6 and 6A** show substantially all of an electronic package covered with a protective covering, according to another embodiment of the invention. **FIG. 6A** shows an enlarged view of a portion of **FIG. 6**.

[0022] **FIG. 7** also shows substantially all of an electronic package covered with a protective covering. A semiconductor chip is wire bonded to the package's substrate.

[0023] **FIG. 8** shows substantially all of an electronic package covered with a protective covering. Solder ball bonding pads are used instead of solder balls, which allows for later installation of solder balls.

[0024] **FIG. 9** shows substantially all of an electronic package covered with a protective covering, except for a plurality of solder ball bonding pads.

DETAILED DESCRIPTION OF TIE PREFERRED EMBODIMENTS

[0025] This invention largely solves the moisture sensitivity problem associated with electronic packages (e.g. chip carriers) by covering substantially all of the external surfaces of the electronic package, with the exception of a portion of the conductors that are required for electrically coupling to an external substrate, with an essentially hermetic covering which is highly hydrophobic. Before sealing with the protective covering, the assembled carrier is preferably heated which removes substantially all of the moisture therein. The protective covering then seals all the surfaces to which it is exposed, forming a barrier which greatly retards future moisture absorption. The reduced level of moisture improves product yields and reliability thru the final assembly and testing processes.

[0026] In one embodiment, all of the package, including all of the external conductor surfaces, are covered (e.g., to facilitate shipment). In another embodiment, portions of the external conductor surfaces are exposed, thus enabling immediate subsequent processing (e.g., solder reflow).

[0027] Similar numbers are used in different FIGS. to indicate similar elements of the invention.

[0028] In the embodiment shown in **FIG. 1**, electronic package **1** is immersed in a solution **2** in order to apply a protective covering thereto. Electronic package 1 comprises a circuit substrate **3** (e.g., a dielectric structure having one/more internal and/or external conductive planes "P" and one more dielectric layers "D"), semiconductor chip **4**, a plurality of conductors **5** electrically coupling semiconductor chip **4** to substrate **3**, and a plurality of conductors **6** for electrically coupling substrate **3** to an external substrate (e.g., a printed circuit board). In one embodiment, conductors **5** and **6** are preferably solder balls which in turn may be of solder compositions (e.g., 90:10 lead:tin, 63:37 lead:tin, etc.) known in the electronic packaging art. Also, these may be of different sizes (e.g., conductors **5** may be of spherical shape having a first diameter while conductors **6**, also spherical, may be of larger diameters. These may also be of different melting points (e.g., those conductors **6** possessing a relatively lower melting point than those coupling the chip to substrate **3**). In **FIG. 1**, a suspending mechanism, such as a dielectric tape **7**, is used to engage conductors **6** and to hold electronic package **1** in solution **2** at the desired level. Tape **7** can act as a suspending mechanism as shown in **FIG. 1**, as a cover layer (described below), or as both a suspending mechanism and as a cover layer as shown in **FIG. 1A**. **FIG.**

1B shows an enlarged portion of electronic package **1** being immersed in solution **2**, using tape **7** as the suspending mechanism.

[0029] Tape **7** is preferably TEFLON with a thickness of 2-4 mils (0.002-0.004 inch). Conductors **6** are preferably depressed partly into tape **7** prior to suspension of electronic package **1** in solution **2**. In this manner, solution **2** is applied to all of the external surfaces of electronic package **1**, except for the portion of conductors **6** suspended above the upper surface of the solution.

[0030] Tape **7** may also act as a cover layer (see below), thereby preventing solution **2** from contacting a predetermined portion of conductors **6**. If conductors **6** are solder balls (e.g., 63:37 lead:tin), then tape **7** could conform to predetermined portions of the outer surfaces of the solder balls, thereby acting as a seal when electronic package **1** is immersed in solution **2**. The solder balls would be depressed into tape **7**, as is seen in **FIG. 1A**

[0031] In the embodiment of **FIG. 1**, solution **2** can be agitated ultrasonically while electronic package **1** is immersed therein. For achieving a desired thickness for the eventual protective covering, it is possible to immerse electronic package **1** a plurality of times (e.g., providing a thickness of 0.001 inch in one embodiment was attainable using a total of four immersions) in a resin/solvent solution containing approximately 10% solids by weight (see more below).

[0032] For ultrasonic application, a frequency in the kilohertz range(e.g., about 55 KHz) is preferred. The device used to provide this may be an ultrasonic bath/cleaner (not shown), of which there are known types in the art.

[0033] Protective covering solution **2** described herein may be any dielectric material that will provide a good hydrophobic barrier for electronic package **1**. Some common solution materials include TEFLON and fluorinated thermosets, which can be applied using one or more of the processes defined herein.

[0034] The preferred TEFLON described for use as solution **2** is more commonly called TEFLON AF, a product of E. I. du Pont de Nemours & Co. Inc. TEFLON AF is a family of amorphous fluoropolymers with glass transition temperatures as high as 300 degrees Celsius based on bis-2,2-trifluoromethyl-4,5-difluoro-1,3-dioxole, and which has unusual properties. The family retains the superior electrical, chemical resistant and thermal properties associated with fluoropolymers. In addition, these polymers have high optical clarity, limited solubility in some commercially available perfluorinated ethers and improved physical properties below the glass transition temperatures. TEFLON AF polymers may be either solution cast into clear micron thin films or melt processed into a variety of forms. TEFLON AF has a very low dielectric constant (1.89-1.93) which decreases with increasing temperature. It also has a constant volume coefficient of thermal expansion below the glass transition temperatures thereof. TEFLON AF also has a high thermal stability (zero weight loss at 260 degrees Celsius). It can be fabricated by spin casting and solution or spray coating from polymer solutions. Using these techniques, it has been possible to obtain clear, substantially pin hole-free film coatings less than one micron thick.

[0035] In addition to package immersion into a solution **2**, other methods of applying the protective covering solution to the electronic package are possible, including spraying or chemical vapor deposition. The coating process can also be completed by brushing. Brushing can be advantageous in that it can allow thicker layers to be deposited in one pass. While TEFLON AF is limited to approximately 10-15% solids, if so applied, solutions of other thermosetting resins such as AROCY F40 available from Ciba-Geigy can be brushed on at up to 50% by weight solids.

[0036] As stated, the protective coating can also be applied by spraying. A suitable solvent/resin solution may be sprayed onto the electronic package, dried, and then heat cured (if necessary). One particular advantage of using TEFLON AF is that it requires no curing step.

[0037] Chemical vapor deposition (CVD) is accomplished by processing the electronic package thru a standard four-stage CVD apparatus, known in the art. The actual coating takes place in the deposition chamber(s) at approximately 0.001 Torr pressure and at 25 degrees Celsius (C.). Examples of solutions which can be satisfactorily applied using such deposition include fluorinated parylene and standard parylene-C type coatings. (Parylene is a known dielectric material in the electronic packaging art.)

[0038] As stated above, curing of the applied coating may be necessary, depending on the material used. Curing offers reduced skin effect and minimal surface coating distortion (see more below). Infrared dry/cure is a preferred method. TEFLON AF can be air dried at room temperature if it is coated from FC-77 fluorocarbon solvent, a known material. Slightly elevated temperatures, e.g., 100 degrees C. for one hour, can be used to accelerate the drying of TEFLON AF. AROCY F-40, with zinc octoate catalyst, should first be dried (typically 20 minutes at 100 degrees C.) and then heated to approximately 280 degrees C. for one hour to achieve full cure. Obviously, prior to heating to this high temperature, any tape should be removed from the electronic package.

[0039] Skin effect occurs when the solution dries at too high a temperature. This causes the outermost portion of the coating to harden before the interior. The outermost layer formed will thus act as a seal before the interior hardens, causing the interior portion of the solution to possibly expand against the sealed (hardened) outer (skin) layer. The result is blistering or voids in the protective covering, thus referred to as skin effect. Significantly, the present process substantially eliminates this occurrence.

[0040] Other curing processes may include air drying and convection heating.

[0041] In the embodiment shown in **FIG. 2**, electronic package **1** is immersed into solution **2** in order to apply a protective covering thereto. In **FIG. 2**, vacuum fixture **14** is used to engage a portion of conductors **6** and to provide a substantially solution-proof seal as the electronic package is immersed. The solution-proof seal keeps solution **2** from contacting those portions of conductors **6** that are engaged by vacuum fixture **14**. In this manner, solution **2** is applied to all of the external surfaces of electronic package **1**, except for the portion of conductors **6** surrounded (sealed) by vacuum fixture **14**. **FIG. 2A** illustrates this form of securement in greater detail.

[0042] Vacuum fixture **14** typically includes a pliable material **15**, such as rubber or vinyl, to engage and conform

to portions of the conductors **6**. The vacuum fixture **14** of **FIG. 2** is intended to engage the portions of the conductors **6** that are to remain free of protective covering during the application process. This engagement forms a seal from which substantially all of the air is removed by vacuum fixture **14**.

[0043] After solution **2** is applied to electronic package **1** through one or more immersions, vacuum fixture **14** is removed, thereby forming electronic package **1** with a dielectric and substantially hydrophobic protective covering over substantially all of the external surfaces of electronic package **1**, except for the portion of conductors **6** that were engaged by the vacuum fixture. Drying and/or curing of the external protective coating material may now occur, depending on the solution composition used.

[0044] The vacuum fixture **14** may also be used when applying any of the solutions to electronic package **1** using one or more of the other various methods disclosed herein. These may include immersion of electronic package **1** into solution **2** with ultrasonic agitation of solution **2**, spraying solution **2** onto electronic package **1**, brushing solution **2** onto electronic package **1**, and chemical vapor deposition of fluorinated parylenes. If the package is to be immersed more than once in the solution, then vacuum figure **14** should remain in place during all such applications.

[0045] In the embodiment shown in **FIG. 3**, electronic package **1** is immersed into solution **2** in order to apply a protective covering thereto. In **FIG. 3**, however, a cover layer **21** is used to cover a portion of conductors **6** and to provide a substantially solution-proof seal of portions of the conductors as the package is immersed. In this manner, solution **2** is applied to all of the external surfaces of electronic package **1**, except for the portion of conductors **6** being sealed by cover layer **21**. **FIG. 3A** is an enlarged view of package **1** being immersed, illustrating the proper positioning of layer **21** in greater detail.

[0046] Cover layer **21** is preferably applied using a masking operation. Some examples of acceptable materials for cover layer **21** include wax, conformal tape (where conductors **6** are depressed into the conformal tape), and photoresist. Typically, the portions of conductors to be used for electrically coupling substrate **3** to an external substrate (e.g., circuit board) are those areas protected by cover layer **21** during the application of solution **2**. In a preferred embodiment, approximately fifty percent of the external surface area of each conductor (preferably a solder ball) was covered (sealed).

[0047] After solution **2** is applied to electronic package **1**, cover layer **21** is removed, thereby forming electronic package **1** with a dielectric and substantially hydrophobic protective covering over substantially all of the external surfaces of the package, except for those portions of conductors **6** that were covered by the cover layer. This package is now ready for shipment and/or subsequent connection (e.g., using solder reflow) to an awaiting circuitized substrate.

[0048] Cover layer **21** may also be applied using one or more of the various disclosed methods cited hereinabove.

[0049] If the solution in **FIG. 3** is to be applied more than once to package **1**, then cover layer **21** should remain in place for all solution immersions. In one embodiment, package **1** was immersed four times, resulting in a satisfactory protective covering thickness of about 0.001 inch.

[0050] In the embodiment shown in **FIG. 4**, electronic package assembly **22** is shown with protective covering **23** applied to substantially all of the external surfaces of electronic package **22**, except for a portion of the plurality of conductors **6**. This resulting structure is, understandably, attainable using any of the processes illustrated in FIGS. **1-3A** and described in detail hereinabove. As stated, electronic package assembly **22** can now be assembled (soldered) onto a printed circuit board PCB, using known solder reflow processing. The printed circuit board can then be assembled into an information handling system (e.g., computer) to form a part thereof. **FIG. 4A** shows a portion of **FIG. 4** in an enlarged view.

[0051] In the embodiment shown in **FIG. 5**, the electronic package assembly **29** is shown with a protective covering **23** applied to substantially all of the external surfaces of the electronic package, again except for a portion of the conductors **6**. In **FIG. 5**, however, the semiconductor chip **4** is wire-bonded (using wiring **9**) to the substrate **3**, after having been positioned within a recess **30** in substrate **3**. It is understood that these wires **9** electrically couple chip contact sites (not shown) to corresponding conductive pads (also not shown) of the circuitry on the substrate's upper surface. As seen in **FIG. 1**, for example, these pads are then coupled (e.g., using plated through holes) to corresponding pads on the substrate's lower surface having the conductors **6** thereon.

[0052] In the embodiment shown in **FIG. 6**, the electronic package assembly **28** is shown with a protective covering **23** applied to substantially all of the external surface of the package. **FIG. 6A** shows a portion of **FIG. 6** in an enlarged view. Chip **4** in **FIG. 6** is electrically coupled to substrate **3** with conductive solder elements **5**. Such a complete covering is attained by totally immersing the package into solution without protecting selected portions of conductors **6**, as occurred in FIGS. **1-3A**. A suitable holder can be used for this.

[0053] In the embodiment shown in **FIG. 7**, the electronic package assembly **30** is shown with a protective covering **23** applied to substantially all of the external surfaces of the electronic package **30**, again including all surfaces of conductors **6**. In **FIG. 7**, as in **FIG. 5**, the semiconductor chip **4** is wire-bonded to the substrate using wiring (e.g., gold) **9**.

[0054] In the embodiments of the invention shown in **FIGS. 6 and 7**, protective covering **23** is applied to all of the external surfaces of the package by any of the methods described above (e.g., such as immersing electronic package **1** without cover layer **21** in solution **2**). Thereafter, selected portions of the protective covering **23** can be removed from at least those portions of the plurality of conductors **6** that are required to electrically couple the substrate with an external substrate. In the meantime, shipping and other handling of the fully protected package assembly is readily possible.

[0055] To remove selected portions of the protective covering, a photoresist may be used. The photoresist may be applied to all portions of the protective covering **23**, except to those selected portions that are to be removed. Then a fluorocarbon solvent, such as the aforementioned FC-77

solvent, may be applied to wash away those portions of covering **23** not protected by the photoresist. Thereafter, the photoresist may or may not be removed from the protective covering **23** before eventual product utilization.

[0056] Since the topography of the underlying solder balls **6** may be somewhat uneven, a liquid or electro-deposited photoresist is preferably used, providing a conformal-type covering on the underlying coating located over balls **6**. Exposure to colluminated light will then image the photoresist, following which imaged portions may be removed.

[0057] It should also be noted that the solder balls **6** need not be applied to the package's substrate before applying the protective covering. In **FIG. 8**, the electronic package is entirely coated with solution and cured. The protective covering is then selectively removed (as described above) so as to expose underlying bonding pads "P" (see also **FIGS. 1 and 1A**) for subsequent solder ball **6** positioning thereon and coupling thereto. The surrounding coating thus facilitates such ball placement by proving a "template" over the exposed pads. The result is seen in **FIG. 9**.

[0058] Alternatively, a mask may be positioned over the solder balls or solder ball bonding pads and the unwanted dielectric removed by exposure to a liquid or air-carried abrasive stream aimed through the mask's holes. Laser ablation may be used to remove the unwanted portions of protective covering **23**. Solder balls **6** may also be bonded using one or more known soldering techniques. For example, the solder balls may be reflowed while located atop the conductors "P".

[0059] The substrates **3** as mentioned above are typically made from known materials such as epoxy resin reinforced with fiberglass (also known as "FR4" in the packaging industry), TEFLON, and ceramic. The conductors **5** and **6**, as mentioned above, are preferably of known solder conducting material, the most preferred being those comprised of lead and tin alloys.

[0060] As further stated above, the conductors **5** that electrically couple the semiconductor chip **4** to the substrate **3** may be of a higher melting point solder material than the conductors **6** used to electrically couple substrate **3** to an external substrate. This is an important feature because, by controlling the reflow temperatures, it allows the solder conductors **6** to reflow when connecting to an external substrate, while at the same time the conductors **5** will be stable, thus keeping intact the required precise electrical coupling between the semiconductor chip **4** and the substrate **3**. By way of specific example, the conductors **5** that electrically couple the semiconductor chip **4** to the substrate **3** can be of the aforementioned 90:10 lead-tin solder which has a melting temperature of approximately 310 degrees C., while the conductors **6** used to electrically couple the substrate **3** to an external substrate can be the aforementioned 63:37 lead-tin, which has a lower melting temperature of approximately 180 degrees C.

[0061] As stated, the conductors **5** that electrically couple the semiconductor chip **4** to the substrate **3** could also be wires **9** as shown in **FIG. 5** and **FIG. 7**. It is further possible to couple leads from substrate **3** (e.g., projecting cantilever leads such as those from a "flexible" substrate made from a dielectric (e.g., polyimide) thin layer having at least one thin layer of circuitry thereon, of which such projecting leads may form a part) to the chip using known thermocompression (application of heat and pressure) bonding.

[0062] Although particular embodiments of the present invention have been shown and described, it will be obvious to those skilled in the art that various changes and modifications may be made therein without departing from the spirit and scope of the present invention.

What is claimed is:

1. A method of providing a protective covering on an electronic package including a substrate, a semiconductor chip positioned on and electrically coupled to said substrate, and a plurality of conductors on said substrate for electrically coupling said substrate to an external substrate, said method comprising covering substantially all of the external surfaces of said substrate, said semiconductor chip and a first portion of the external surface of said conductors with a protective covering.

2. The method of claim 1, further comprising providing a cover layer on at least a second portion of the external surfaces of said conductors to prevent covering thereof with said protective covering.

3. The method of claim 2, wherein said providing of said cover layer onto said second portions of said conductors is accomplished using a masking operation.

4. The method in claim 3, wherein said masking operation comprises covering said second portions of said conductors with wax, conformal tape, or photoresist.

5. The method of claim 4, further comprising depressing at least said second portions of said conductors into said cover layer prior to said covering of said first portions of said conductors.

6. The method of claim 2, wherein said masking operation further includes using a vacuum fixture to engage said second portions of said conductors to prevent covering thereof with said protective covering.

7. The method of claim 6, wherein said vacuum fixture further comprises engaging said second portions of said conductors with rubber or vinyl material.

8. The method of claim 1, wherein at least a portion of said protective covering on said electronic package is applied by spraying.

9. The method of claim 1, wherein at least a portion of said protective covering on said electronic package is applied by brushing.

10. The method of claim 1, wherein at least a portion of said protective covering on said electronic package is applied by vapor deposition.

11. The method of claim 1, wherein at least a portion of said protective covering on said electronic package is applied by immersing said electronic package in a solution.

12. The method of claim 11, further comprising controlling the depth that said electronic package is immersed in said solution.

13. The method of claim 11, wherein said electronic package is immersed in a solution of TEFLON or a fluorinated thermosetting material.

14. The method of claim 11, wherein said electronic package is immersed in said solution using a tape as a suspending mechanism, said tape engaging said conductors.

15. The method of claim 14, wherein said conductors are depressed into said tape prior to said immersing and remain so depressed during said immersing.

16. The method of claim 11, wherein said solution is agitated ultrasonically when said electronic package is immersed in said solution.

17. The method of claim 11, wherein said electronic package is immersed a plurality of times within said solution.

18. The method of claim 11, further comprising curing said protective covering.

19. The method of claim 18, wherein said curing is accomplished by infrared heating.

20. The method of claim 18, wherein said curing is accomplished by air drying.

21. The method of claim 18, wherein said curing is accomplished by convection heating.

22. A method of providing a protective covering on an electronic package including a substrate having a plurality of conductors for electrically coupling said substrate to an external substrate, a semiconductor chip positioned on and electrically connected to said substrate, said method comprising covering substantially all of the external surfaces of said substrate, said semiconductor chip, and said plurality of conductors with a protective covering, and thereafter removing selected portions of said protective covering from said plurality of conductors.

23. The method of claim 22, further including bonding a conductor element to at least one of said conductors after removal of said portions of said protective covering.

24. The method of claim 22, wherein at least a portion of said protective covering on said electronic package is applied by spraying.

25. The method of claim 22, wherein at least a portion of said protective covering on said electronic package is applied by brushing.

26. The method of claim 22, wherein at least a portion of said protective covering on said electronic package is applied by vapor deposition.

27. The method of claim 22, wherein at least a portion of said protective covering on said electronic package is applied by immersing said electronic package in a solution.

28. The method of claim 27, wherein said solution is TEFLON or a fluorinated thermosetting material.

29. The method of claim 27, wherein said solution is agitated ultrasonically when said electronic package is immersed in said solution.

30. The method in claim 27, wherein said electronic package is immersed a plurality of times within said solution.

31. The method of claim 27, further comprising curing said protective covering.

32. The method of claim 31, wherein said curing is accomplished by infrared heating.

33. The method of claim 31, wherein said curing is accomplished by air drying.

34. The method of claim 31, wherein said curing is accomplished by convection heating.

35. An electronic package comprising:

a first circuitized substrate having first and second surfaces;

a semiconductor chip positioned on said first surface of said first substrate and electrically coupled thereto;

a first plurality of conductors located on said second surface of said first circuitized substrate and adapted for electrically coupling said first circuitized substrate to an external circuitized substrate; and

a dielectric protective covering, substantially covering all of the external surfaces of said electronic package, except for at portion of selected ones of said plurality of conductors.

36. The electronic package of claim 35, wherein said dielectric protective covering forms a hydrophobic barrier.

37. The electronic package of claim 35, wherein said dielectric protective covering is comprised of TEFLON AF, a fluorinated thermosetting material or a fluorinated parylene material.

38. The electronic package of claim 35, wherein said first circuitized substrate is comprised of polymer or ceramic material and further includes one or more conductive layers.

39. An electronic package of claim 35, wherein said first plurality of conductors are comprised of solder material.

40. The electronic package of claim 35, further including a second plurality of conductors for electrically coupling said semiconductor chip to said first circuitized substrate.

41. The electronic package of claim 40, wherein said second plurality of conductors comprise a plurality of conductive wires.

42. The electronic package of claim 40, wherein said second plurality of conductors are comprised of solder material.

43. The electronic package of claim 42, wherein said first plurality of conductors are comprised of a first solder material and said second plurality of conductors are comprised of a second, different solder material, said first and second solder materials having different melting points.

44. The electronic package of claim 43, wherein said second plurality of conductors for electrically coupling said semiconductor chip to said first circuitized substrate are comprised of 90:10 lead-tin solder or 97:3 lead-tin solder.

45. The electronic package of claim 44, wherein said first plurality of conductors located on said substrate for electrically coupling said substrate to an external substrate are comprised of 63:37 lead-tin solder.

46. An electronic package comprising:

a first circuitized substrate having first and second surfaces;

a semiconductor chip positioned on said first surface of said first substrate and electrically coupled thereto;

a first plurality of conductors located on said second surface of said first circuitized substrate for electrically coupling said substrate to an external second substrate; and

a dielectric protective covering, substantially covering all of the external surfaces of said electronic package, including said conductors.

47. The electronic package of claim 46, wherein said dielectric protective covering forms a hydrophobic barrier.

48. The electronic package of claim 47, wherein said dielectric protective covering is comprised of TEFLON AF, a fluorinated thermosetting material or a fluorinated parylene material.

49. The electronic package of claim 46, wherein said first circuitized substrate is comprised of polymer or ceramic material and further includes one or more conductive layers.

50. The electronic package of claim 46, wherein said first plurality of conductors are comprised of solder material.

51. The electronic package of claim 46, further including a second plurality of conductors for electrically coupling said semiconductor chip to said first circuitized substrate.

52. The electronic package of claim 51, wherein said second plurality of conductors comprises a plurality of conductive wires.

53. The electronic package of claim 51, wherein said second plurality of conductors are comprised of solder material.

54. The electronic package of claim 51, wherein said first plurality of conductors are comprised of a first solder material and said second plurality of conductors are comprised of a second solder material, said first and second solder materials having different melting points.

55. The electronic package of claim 54, wherein said second plurality of conductors for electrically coupling said semiconductor chip to said first circuitized substrate are comprised of 90:10 lead-tin solder or 97:3 lead-tin solder.

56. The electronic package of **55**, wherein said plurality of conductors located on said substrate for electrically coupling said substrate to an external circuitized substrate are comprised of 63:37 lead-tin solder.

* * * * *

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United States Patent [19]

Lee et al.

[11] Patent Number: 5,894,107

[45] Date of Patent: Apr. 13, 1999

[54] **CHIP-SIZE PACKAGE (CSP) USING A MULTI-LAYER LAMINATED LEAD FRAME**

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[73] Assignee: **Samsung Electronics Co., Ltd.**, Suwon-city, Rep. of Korea

[21] Appl. No.: **08/904,756**

[22] Filed: **Aug. 1, 1997**

[30] **Foreign Application Priority Data**

Aug. 19, 1996 [KR] Rep. of Korea 96-34274

[51] **Int. Cl.**[6] **H01L 23/28**

[52] **U.S. Cl.** **174/52.2**; 174/52.4; 257/676; 257/693; 257/738; 257/778; 257/787

[58] **Field of Search** 257/676, 778, 257/669, 672, 673, 674, 666, 737, 738, 693, 787; 174/52.4, 52.2

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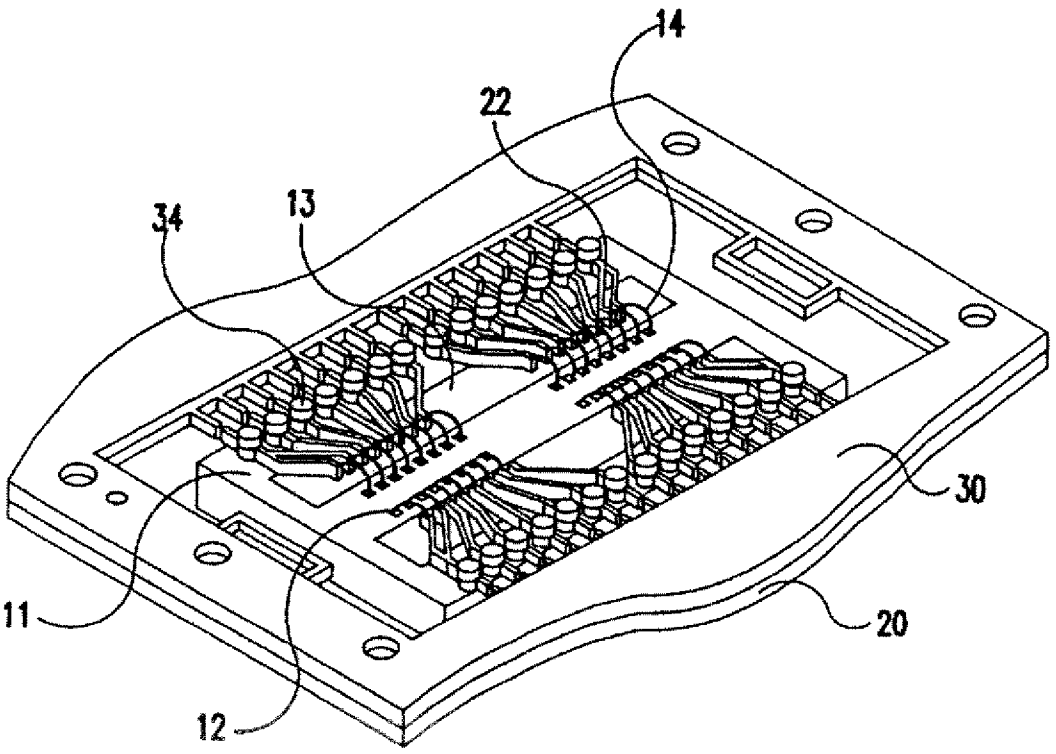
Primary Examiner—Kristine Kincaid
Assistant Examiner—Hung V. Ngo
Attorney, Agent, or Firm—Jones & Volentine, L.L.P.

[57] **ABSTRACT**

A method for manufacturing a chip-size package and the chip-size package produced by the method uses first and second lead frames which are prepared by a stamping process. The first lead frame has leads with receiving parts, and the leads are integrally formed with lengthwise side rails of the lead frame. The second lead frame has external connections which align with the receiving parts of the leads when the second lead frame is positioned on top of the first lead frame and attached thereto. Guide holes located on the crosswise side rails of both lead frames can be used to easily align the two lead frames. A semiconductor chip is then adhered to the underside of the first lead frame, and the bonding pads of the semiconductor chip are electrically connected to the leads of the first lead frame. Then the two lead frames and the chip are encapsulated, with only the external connections of the second lead frame remaining exposed to the outside. Solder balls are then attached to the external connections for mounting onto a substrate. This chip-size package is inexpensive to produce, because the first and second lead frames can be produced by a stamping process, which is less complex and cheaper than the conventional half-etching process.

9 Claims, 6 Drawing Sheets



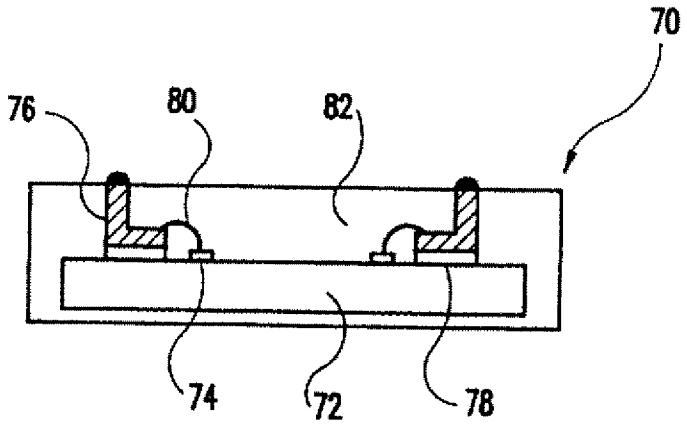


FIG.1
PRIOR ART

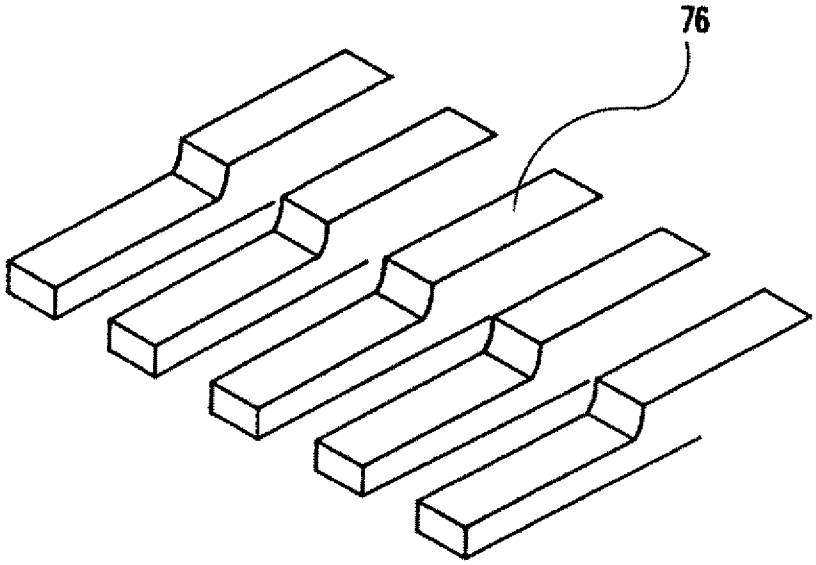


FIG.2
PRIOR ART

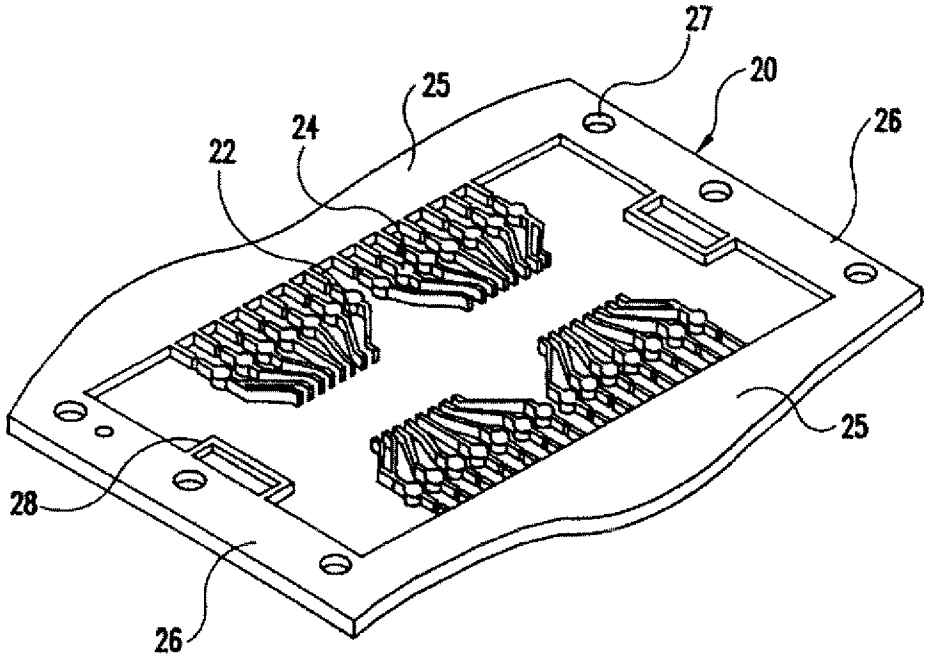


FIG.3

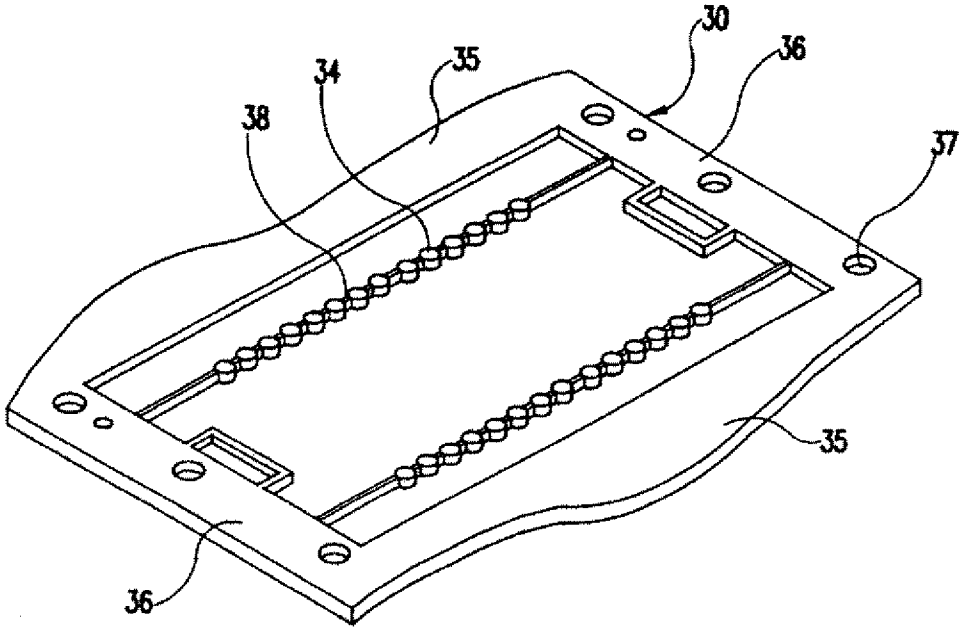


FIG.4

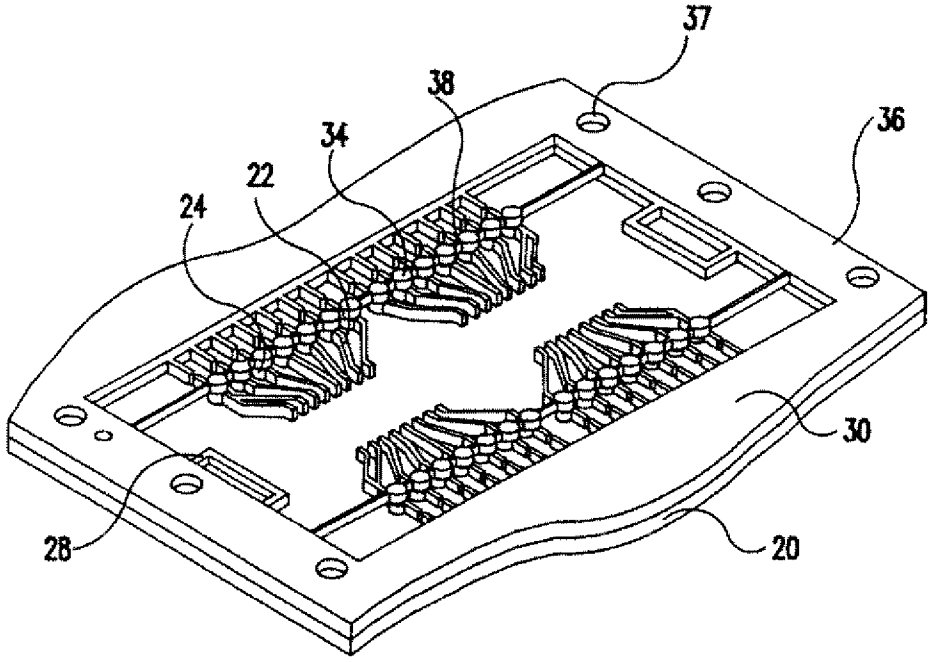


FIG.5

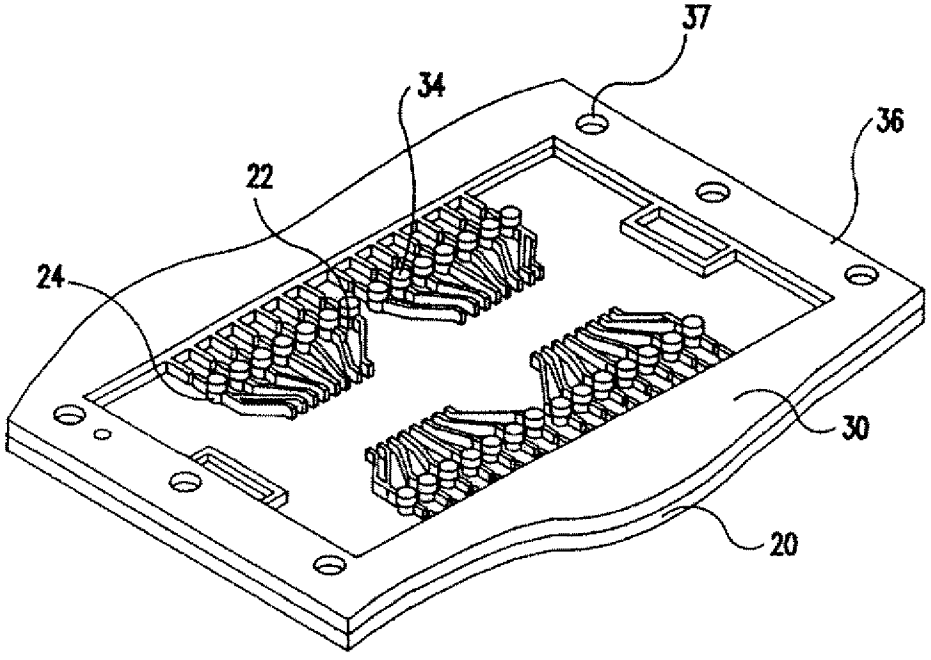


FIG.6

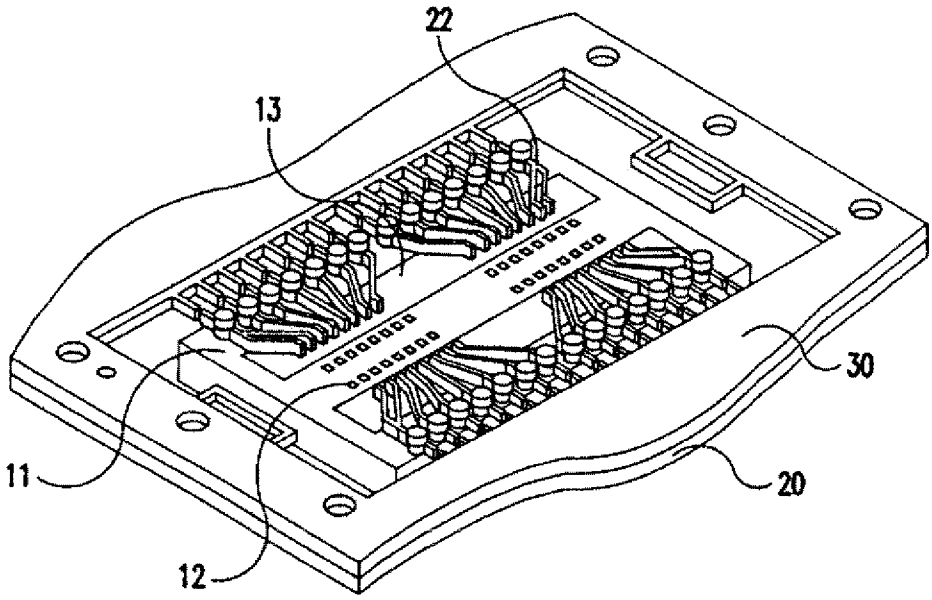


FIG.7

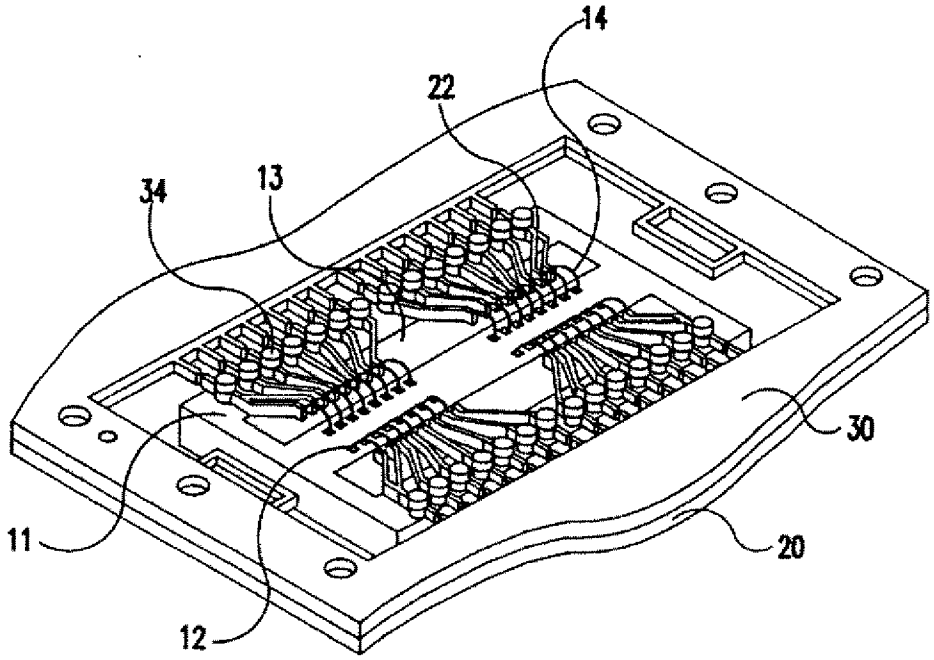


FIG.8

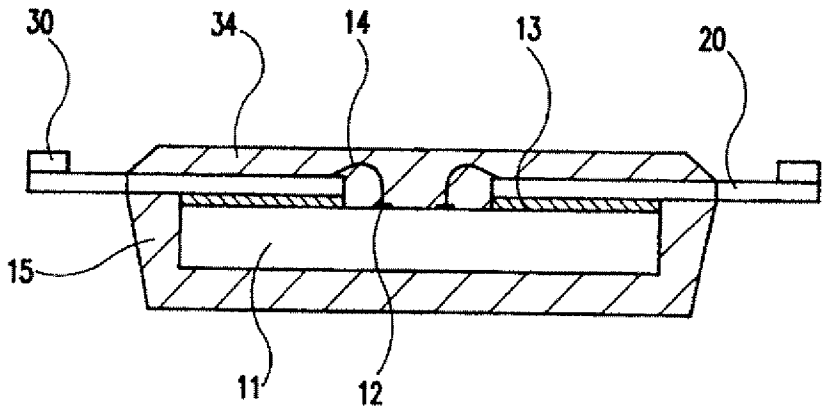


FIG.9

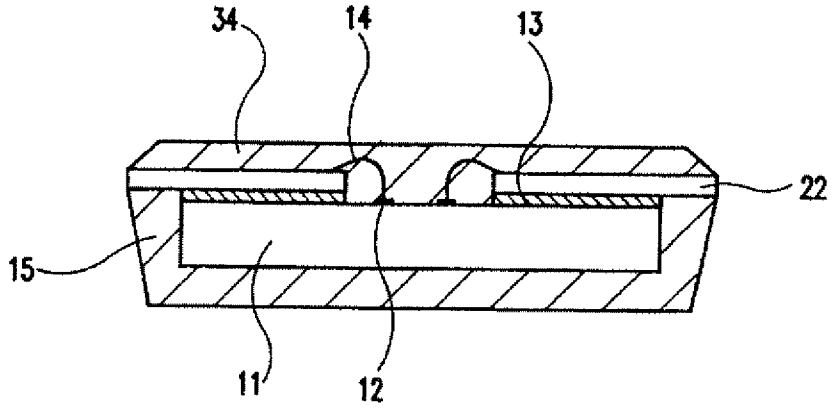


FIG.10

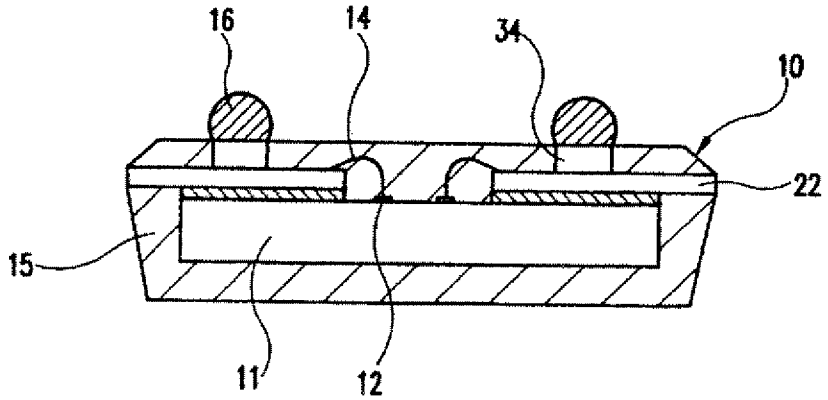


FIG.11

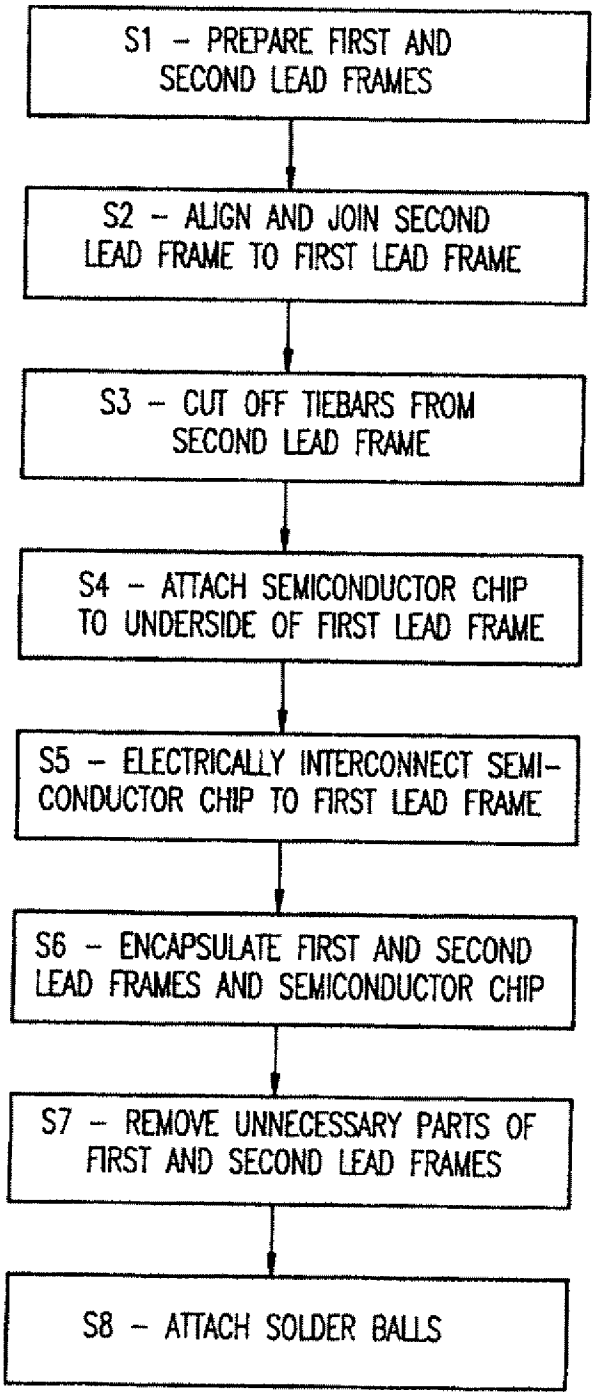

S1 – PREPARE FIRST AND SECOND LEAD FRAMES
S2 – ALIGN AND JOIN SECOND LEAD FRAME TO FIRST LEAD FRAME
S3 – CUT OFF TIEBARS FROM SECOND LEAD FRAME
S4 – ATTACH SEMICONDUCTOR CHIP TO UNDERSIDE OF FIRST LEAD FRAME
S5 – ELECTRICALLY INTERCONNECT SEMI-CONDUCTOR CHIP TO FIRST LEAD FRAME
S6 – ENCAPSULATE FIRST AND SECOND LEAD FRAMES AND SEMICONDUCTOR CHIP
S7 – REMOVE UNNECESSARY PARTS OF FIRST AND SECOND LEAD FRAMES
S8 – ATTACH SOLDER BALLS

FIG.12

CHIP-SIZE PACKAGE (CSP) USING A MULTI-LAYER LAMINATED LEAD FRAME

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention generally relates to a method for manufacturing a chip-size package (CSP), and the chip-size package produced by the method, and more particularly to a method for manufacturing a chip-size package using a multi-layer laminated lead frame.

2. Background of the Related Art

The miniaturization and multi-funtionalization of electronic equipment has resulted in the advancement of manufacturing technologies for semiconductor devices. This advancement includes progress in packaging technology toward high mounting density, high processing speed and miniaturization.

The mounting density of the chip package on a substrate has gradually increased, as the structure of the package has changed from the insert mounting type to the surface mounting type (SMT).

Due to this recent trend toward high mounting density of the package on a substrate, the kind of package has been changed from dual inline package (DIP) to small outline package (SOP), and then to thin small outline package (TSOP) whose thickness is as small as one-half that of a conventional SOP.

Particularly, in the case of the memory semiconductor chip, the size of the semiconductor chip increases as the capacity increases. If the size of the semiconductor chip increases, it is difficult to meet the reliability requirement of the package with the conventional plastic package technology.

Accordingly, a so-called chip-size package which has the same size or is slightly larger than the chip itself has been developed to satisfy this need.

The chip-size package has some advantages in that it is smaller and thinner than any other package type, it provides better electrical performance than most SMT packages due to shorter leads and lower lead inductance, and that it is easier to handle than a bare chip.

Many semiconductor manufacturers are developing various types of chip-size packages. The chip-size packages are classified into flexible circuit interposer type, rigid substrate interposer type, transfer molded, type, custom lead frame type, and TCP (Tape Carrier Package) type. Among these chip-size packages, the chip-size package employing LOC (Lead On Chip) technology can meet the demand for high density of the package.

An example of the chip-size package employing LOC technology is as follows. FIG. **1** is a cross-sectional view showing an example of the chip-size package employing the LOC technology, and FIG. **2** is an enlarged view of the lead portions of the chip-size package in FIG. **1**.

Referring to FIG. **1** and FIG. **2**, an active surface of the semiconductor chip **72** is attached to the lower surface of the leads **76** by using a double-sided adhesive tape **78** in the chip-size package **70**. Because the upper surfaces of the leads **76** were partially etched by the half-etching method in the manufacturing process of the lead frame, the inner portions of the leads **76** are thin and the outer portions of the leads **76** are thick. Accordingly, the leads **76** are L-shaped.

The upper surfaces of the thin portions of the leads **76** and the bonding pads **74** of the semiconductor chip **72** are

electrically interconnected by gold (Au) wires **80**. The semiconductor chip **72** and the leads **76** including the bonding pads **74** and the gold wires **80** are encapsulated with an epoxy molding compound **82** so that the semiconductor chip **72** and the gold wires **80** are protected from the external environment, and the upper surfaces of the thick portions of the leads **76** are exposed to the outside for the next level electrical connection such as mounting to a substrate.

The conventional chip-size package using the lead frame which is manufactured by using the half-etching method as shown above has at least one drawback, in that the manufacturing process of the lead frame is complicated and expensive, compared to a lead frame which is manufactured by using a stamping method.

SUMMARY OF THE INVENTION

Accordingly, an object of the present invention is to provide a simplified chip-size package and a simplified method for manufacturing the chip-size package using a lead frame, which has a reduced manufacturing cost since the lead frame is manufactured using a stamping method.

The foregoing object can be achieved by a method for manufacturing a chip-size package, which comprises the steps of:

preparing a first lead frame and a second lead frame by a stamping process, the first lead frame having a plurality of rows of leads having receiving parts, the leads being integrally formed with the lengthwise side rails of the first lead frame, and the second lead frame having a plurality of rows of external connection means extending parallel to the lengthwise side rails of the second lead frame, the rows of external connection means being attached to the crosswise side rails of the second lead frame using tiebars;

aligning the first lead frame to the second lead frame by aligning corresponding guide holes located on the crosswise side rails of the first and second lead frames, and joining the second lead frame to the first lead frame by a welding or soldering process such that the receiving parts of the leads of the first lead frame are aligned with and located beneath the external connection means of the second lead frame;

cutting off the tiebars which had secured the rows of external connection means in place on the second lead frame by using a punching method;

attaching a semiconductor chip having a plurality of bonding pads on its active surface to the leads of the first lead frame by using an adhesive means;

electrically interconnecting the bonding pads of the semiconductor chip to the inner ends of the leads of the first lead frame using a wire-bonding method;

encapsulating the entire assembly in an encapsulant, with the upper surfaces of the external connection means exposed to the outside;

cutting off unnecessary parts of the first and second lead frames using a punching method; and

attaching solder balls to the exposed upper surfaces of the external connection means.

BRIEF DESCRIPTION OF THE ATTACHED DRAWINGS

These and various other features and advantages of the present invention will be readily understood with reference to the following detailed description taken in conjunction with the accompanying drawings, wherein like reference numerals designate like structural elements, and, in which:

FIG. 1 is a cross-sectional view showing an example of the conventional chip-size package employing LOC technology;

FIG. 2 is an enlarged view of the lead portions of the chip-size package as shown in FIG. 1;

FIG. 3 is a perspective view showing the first lead frame according to the present invention;

FIG. 4 is a perspective view showing the second lead frame according to the present invention;

FIG. 5 is a perspective view showing the second lead frame of FIG. 4 joined to the first lead frame of FIG. 3;

FIG. 6 is a perspective view showing the first and second lead frames of FIG. 5 with the tiebars cut off of the second lead frame;

FIG. 7 is a perspective view showing the active surface of the semiconductor chip attached to the lower surface of the first lead frame;

FIG. 8 is a perspective view showing the assembly of FIG. 7, after wire-bonding;

FIG. 9 is a cross-sectional view showing the semiconductor chip, the first lead frame and the second lead frame including the bonding pads and the bonding wires of FIG. 8 encapsulated with an encapsulant;

FIG. 10 is a cross-sectional view showing the encapsulated assembly of FIG. 9, with the unnecessary parts of the first lead frame and the second lead frame cut off;

FIG. 11 is a cross-sectional view showing solder balls attached to the exposed upper surfaces of the external connection means of the encapsulated assembly of FIG. 10; and,

FIG. 12 is a flow chart illustrating the steps of the method for manufacturing the chip-size package of the present invention.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENT

A preferred embodiment of the present invention will be described below with reference to the accompanying drawings.

FIG. 3 to FIG. 11 are the views showing the results of each step in the manufacturing process of a chip-size package according to the present invention.

FIG. 12 is a flow chart showing the manufacturing steps of the method for producing the chip-size package shown in FIGS. 3–11.

A first lead frame 20 and a second lead frame 30 are prepared using a stamping method. Referring to FIG. 3 and FIG. 4, the first lead frame 20 comprises a pair of crosswise side rails 26, a pair of lengthwise side rails 25, and a plurality of leads 22 equally spaced at a designated distance along the lengthwise side rails 25.

The leads 22 are formed in two rows, each row extending inwardly toward the other row from one of the lengthwise side rails 25. The inner ends of the leads 22 arranged in one row are separated a designated distance from the inner ends of the leads 22 arranged in the other row.

The outer ends of the respective leads 22 are connected with the two lengthwise side rails 25 of the first lead frame 20 for providing mechanical support. Each lead 22 is integrally formed with a receiving part 24 which is formed in a disk shape and which is disposed at an approximate middle of the lead 22. Crosswise side rails 26 connect lengthwise side rails 25 together at either end of the rows of leads 22. Guide through-holes 27 are formed in the crosswise side rails 26. A tiebar 28 is formed on each crosswise side rail 26 as shown in FIG. 3.

Second lead frame 30 comprises a pair of lengthwise side rails 35 and a pair of crosswise side rails 36, similar to first lead frame 20. A plurality of external connection means 34 are formed in two rows and are connected to each other by tiebars 38. An end of each tiebar 38 is attached to one of the crosswise side rails 36, such that each row of external connection means 34 is spaced parallel to and at a designated distance from the lengthwise side rails 35. Each one of the external connection means 34 is formed in a disk shape, and one row of external connection means 34 is separated from the other row of external connection means 34 by a designated distance.

The size of the second lead frame 30 is the same as that of the first lead frame 20, and when the second lead frame 30 is placed on top of the first lead frame 20, the rows of external connection means 34 of the second lead frame 30 are disposed on top of the receiving parts 24 of the first lead frame 20. Crosswise side rails 36 connect lengthwise side rails 35 together, and guide through-holes 37 are formed in the crosswise side rails 36.

The diameter of each disk of the external connection means 34 of the second lead frame 30 is equal to or larger than the diameter of each disk of the receiving parts 24 of the first lead frame 20. This insures that a punching means (not shown) used to cut off the tiebars 38 will not damage the receiving parts 24 of the first lead frame 20. The external connection means 34 of the second lead frame 30 are spaced apart from one another the same distance that the receiving parts 24 of the first lead frame 20 are spaced apart from one another.

Further, the guide through-holes 37 in second lead from 30 are disposed on a position corresponding to the guide through-holes 27 in the first lead frame 20, and the size and the shape of the guide through-holes 37 are the same as those of the guide through-holes 27.

FIG. 5 shows the second lead frame 30 aligned on top of the first lead frame 20. The second lead frame 30 and the first lead frame 20 are joined by welding or soldering so that the external connection means 34 of the second lead frame 30 are aligned and joined to the corresponding receiving parts 24 of the first lead frame 20. If the guide through-holes 37 of the second lead frame 30 and the guide through-holes 27 of the first lead frame 20 are exactly aligned, the external connection means 34 of the second lead frame 30 can be aligned on top of the receiving parts 24 of the first lead frame 20.

FIG. 6 shows the assembly of FIG. 5 after cutting off the tiebars 38 from the second lead frame 30. The tiebars 38 of the second lead frame 30 are cut off by using a punching means (not shown). At this time, the punching means does not damage the receiving parts 24 of the first lead frame 20, because the external connection means 34 covers the receiving parts 24 of the first lead frame 20. After tiebars 38 are cut off, the external connection means 34 of the second lead frame 30 are aligned on the corresponding receiving parts 24 of the first lead frame 20.

FIG. 7 shows a semiconductor chip 11 attached to the first lead frame 20 by using an adhesive means such as a double-sided adhesive polyimide tape or a non-conductive adhesive 13. On the semiconductor chip 11, the bonding pads 12 are disposed in two rows at a central region of an active surface of the chip. One surface of the double-sided adhesive polyimide tape 13 is attached to the lower surface of the first lead frame 20 by thermocompression bonding.

Then, the other surface of the double-sided adhesive polyimide tape **13** is attached to the active surface of the semiconductor chip **11** by thermocompression with the exposed bonding pads **12**. At this time, a non-conductive adhesive may be used instead of the double-sided adhesive polyimide tape **13**.

FIG. **8** shows the assembly of FIG. **7** with bonding wires **14** connecting the bonding pads **12** of the chip **11** to the leads **22** of the first lead frame **20**. The bonding pads **12** disposed at the central region of the active surface of the semiconductor chip **11** and the inner ends of the corresponding leads **22** are electrically interconnected by bonding wires, e.g. gold wires **14**. The bonding pads **12** of the semiconductor chip **11** and the external connection means **34** of the second lead frame **30** are thereby electrically interconnected by a wire-bonding technique. It is possible to employ various techniques such as a bump bonding or a bonding method like TAB bonding for electrically connecting the bonding pads **12** to the leads **22** of first lead frame **20**.

FIG. **9** shows a cross-sectional view of the assembly of FIG. **8** after encapsulation, so that the upper surfaces of the external connection means **34** are exposed toward the outside for electrical connection to the external interconnections. The semiconductor chip **11**, the first lead frame **20** and the second lead frame **30** including the bonding pads **12** and the gold wires **14** are encapsulated with an encapsulant such as an epoxy molding compound **15** (hereinafter referred to as "EMC"), in order to protect them from the external environment.

FIG. **10** shows the assembly of FIG. **9** after the unnecessary parts of the first lead frame **20** and the second lead frame **30** have been cut off. The lead portions of the first lead frame **20** which protrude from the encapsulated package body are cut off by using the punching means after the encapsulation step. At the same time, the lead portions of the second lead frame **30** which protrude from the encapsulated package body are also cut off .

FIG. **11** shows the assembly of FIG. **10** after solder balls have been attached to the package. The metal balls, e.g. solder balls **16**, are attached to the exposed upper surfaces of the external connection means **34** of the second lead frame **30** for an easy mounting onto a substrate (not shown).

The method for manufacturing the chip-size package as described above is illustrated in the flow chart of FIG. **12**. The manufacturing steps are as follows: (1) preparing a first lead frame and a second lead frame by a stamping process (S1), the first lead frame having a plurality of rows of leads having receiving parts, the leads and the receiving parts being integrally formed with each other and with the lengthwise side rails of the lead frame, the second lead frame having a plurality of rows of external connection means extending parallel to the lengthwise side rails of the lead frame, the rows of external connection means being attached to the crosswise side rails of the second lead frame with tiebars; (2) aligning the first lead frame to the second lead frame by aligning corresponding guide holes located on the crosswise side rails of the first and second lead frames, and joining the first lead frame to the second lead frame by a welding or soldering process, such that the receiving parts of the leads of the first lead frame are aligned with and located beneath the external connection means of the second lead frame (S2); (3) cutting off the tiebars which had secured the rows of external connection means in place on the second lead frame by using a punching method (S3); (4) attaching a semiconductor chip having a plurality of bonding pads on its active surface to the leads of the first lead frame by using an adhesive means (S4); (5) electrically interconnecting the bonding pads of the semiconductor chip to the inner ends of the leads of the first lead frame using a wire-bonding method (S5); (6) encapsulating the entire assembly in an encapsulant, with the upper surface of the external connection means exposed to the outside (S6); (7) cutting off unnecessaary parts of the first and second lead frames using a punching method (S7); and (8) attaching solder balls to the exposed upper surfaces of the external connection means (S8).

With the present invention, it is possible to simplify the package manufacturing process by employing lead frames which can be easily manufactured by a stamping method instead of an etching method, and to use existing manufacturing facilities to manufacture the package.

Further, it is possible to reduce the package manufacturing cost, since a stamping method is less expensive than an etching method in terms of the manufacturing cost of the lead frame.

Thus, the present invention has advantages that chip-size packages can be manufactured by a simple and inexpensive manufacturing process using existing facilities.

Although a preferred embodiment of the present invention has been described in detail hereinabove, it should be clearly understood that many variations and/or modifications of the basic inventive concepts herein taught which may appear to those skilled in the art will still fall within the spirit and scope of the present invention as defined in the appended claims.

What is claimed is:

1. A chip-size package comprising:

a first lead frame having a pair of lengthwise side rails and a pair of crosswise side rails, a plurality of rows of leads having receiving parts, the leads and receiving parts integrally formed with each other and with the lengthwise side rails, and a plurality of guide holes formed in the crosswise side rails;

a second lead frame aligned above and joined to the first lead frame, the second lead frame having a pair of lengthwise side rails and a pair of crosswise side rails, a plurality of rows of external connection means located parallel to the lengthwise side rails and aligned above the receiving parts of the plurality of rows of leads on the first lead frame, and a plurality of guide holes formed in the crosswise side rails aligned with the guide holes in the first lead frame; and

a semiconductor chip having a plurality of bonding pads on an active surface thereof and bonded to an underside of the first lead frame, the bonding pads of the semiconductor chip being electrically interconnected with inner ends of the leads of the first lead frame;

said first and second lead frames and said semiconductor chip being encapculated as an assembly, such that an upper surface of the external connection means is exposed to outside.

2. The chip-size package of claim **1**, further comprising solder balls attached to the exposed upper surface of the external connection means.

3. The chip-size package of claim **1**, wherein each one of the external connection means of the second lead frame is larger than or the same size as each one of the receiving parts of the leads of the first lead frame.

4. The chip-size package of claim **1**, wherein the electrical interconnection between the bonding pads of the semicon-

ductor chip and the inner ends of the leads of the first lead frame is formed by a wire-bond.

5. The chip-size package of claim 1, wherein the electrical interconnection between the bonding pads of the semiconductor chip and the inner ends of the leads of the first lead frame is formed by TAB (tape automated bonding).

6. The chip-size package of claim 1, wherein the electrical interconnection between the bonding pads of the semiconductor chip and the inner ends of the leads of the first lead frame is formed by bump bonding.

7. The chip-size package of claim 1, wherein the semiconductor chip is adhered to the underside of the first lead frame by a double-sided adhesive polyimide tape.

8. The chip-size package of claim 1, wherein the semiconductor chip is adhered to the underside of the first lead frame by a non-conductive adhesive.

9. The chip-size package of claim 1, wherein the semiconductor chip, and first and second lead frames are encapsulated using an epoxy molding compound.

* * * * *

RELATED PROCEEDINGS APPENDIX

U.S. Patent Application No. 09/483,712

Filed January 14, 2000

Copy of Decision On Appeal Mailed November 19, 2004

The opinion in support of the decision being entered today was **not** written for publication and is **not** binding precedent of the Board.

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte TONGBI JIANG and EDWARD A. SCHROCK

Appeal No. 2004-2144
Application No. 09/483,712

ON BRIEF

Before WALTZ, DELMENDO, and PAWLIKOWSKI, Administrative Patent Judges.

WALTZ, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on an appeal from the primary examiner's final rejection of claims 1 through 20. The remaining claims in this application are claims 21 through 29, which stand withdrawn from further consideration as directed to a non-elected invention (Brief, page 2). We have jurisdiction pursuant to 35 U.S.C. § 134.

According to appellants, the invention is directed to chip-scale semiconductor packages in a ball grid array configuration using a lead frame as an interposer (Brief, page 3). A further

understanding of the invention may be gleaned from representative independent claim 1, as reproduced below:

1. A chip-scale package comprising:

a semiconductor die having an active surface having at least one bond pad thereon;

at least one conductive trace spaced from said at least one bond pad and having an upper surface and a lower surface, the lower surface of said at least one conductive trace substantially non-conductively attached to a portion of the active surface of said semiconductor die;

at least one discrete conductive bond member connecting the at least one conductive trace to the at least one bond pad on the active surface of said semiconductor die;

at least one carrier bond attached to the upper surface of the at least one conductive trace; and

an encapsulant material encapsulating said semiconductor die, the at least one conductive trace, the at least one discrete conductive bond and a portion of the at least one carrier bond, the at least one carrier bond having another portion extending beyond said encapsulant material.

Appellants state that the claims do not stand or fall together (Brief, page 4), contrary to the examiner's statement (Answer, page 3, ¶(7); see the Reply Brief, page 2). Since appellants provide reasonably specific, substantive arguments for the patentability of individual claims 3, 6, 11, 12 and 14 (Brief, page 9), we consider these claims separately while the remaining claims stand or fall together. See 37 CFR

§ 1.192(c)(7)(2002); *In re McDaniel*, 293 F.3d 1379, 1383, 63 USPQ2d 1462, 1465 (Fed. Cir. 2002).

The examiner has relied upon the following references as evidence of obviousness:

Lee et al. (Lee)	5,894,107	Apr. 13, 1999
Farnworth	6,147,413	Nov. 14, 2000 (filed Aug. 7, 1997)

The claims on appeal stand rejected under 35 U.S.C. § 103(a) as unpatentable over Farnworth in view of Lee (Answer, page 3). We *affirm* the examiner's rejection on appeal essentially for the reasons stated in the Answer and those reasons set forth below.

OPINION

The examiner finds that Farnworth discloses a chip scale package comprising a semiconductor die (1004) having an active surface, a plurality of bond pads (1002), with the lower surface of a dielectric element (1006) attached to a portion of the active surface of the die (Answer, page 4). The examiner also finds that the lower surface of a plurality of conductive traces (1016) is attached to the upper surface of the dielectric element (1006), with conductive bond members connecting each conductive trace to the bond pads (*id.*). The examiner further finds that carrier bonds (1032) are disposed on an upper surface of the conductive trace and an encapsulating material (1018) covers

portions of the die, the dielectric element, the conductive traces, the bond members and the carrier bonds (*id.*). The examiner recognizes that Farnworth discloses all of the claimed elements except the discrete conductive bond connecting the conductive trace to the bond pad (*id.*). Therefore the examiner applies Lee to show a similar chip-size package[1] in which a conductive trace is spaced from a bond pad, with a discrete conductive bond in the form of a wire connecting the conductive trace to a bond pad formed on the surface of a semiconductor chip (*id.*).[2] From these findings, the examiner concludes that it would have been obvious to one of ordinary skill in the art at the time the invention was made to employ the discrete conductive

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[1]In the event of further or continuing prosecution of this application, the examiner and appellants should consider whether Lee alone discloses structures meeting the claimed limitations (i.e., see Figures 9-11).

[2]The examiner states that the use of discrete electrical bonds (lead or bond wires) was "notoriously well known" in the art, as evidenced by appellants' Figure 1 which is listed as "Prior Art" (Answer, page 5). We also note that Figure 1 of Lee is labeled as "PRIOR ART" and contains bond wires 80 connecting bonding pad 74 to lead 76. It is axiomatic that admitted prior art in an applicant's specification may be used in determining the patentability of a claimed invention (*In re Nomiya*, 509 F.2d 566, 570-71, 184 USPQ 607, 611-12 (CCPA 1975); and that consideration of the prior art cited by the examiner may include consideration of the admitted prior art found in an applicant's specification (*In re Davis*, 305 F.2d 501, 503, 134 USPQ 256, 258 (CCPA 1962); *cf.*, *In re Hedges*, 783 F.2d 1038, 1039-40, 228 USPQ 685, 686 (Fed. Cir. 1986)).

bonds in the form of wires in the configuration of Farnworth for the benefits taught by Lee, namely to provide the advantage of smaller packages, better electrical performance and higher package density (Answer, page 5). We agree.

Appellants argue that the fact that bond wires such as those taught by Lee are known in the art does not mean that bond wires may be incorporated into the structure disclosed by Farnworth (Brief, page 6). Appellants argue that, due to the differences in structure and scale between the repattern traces of Farnworth and the wires of Lee, there is no support for the examiner's proposed modification (Brief, page 7). Appellants further argue that adding bond wires to the repattern structure of Farnworth would require an enlarged packaged size, would decrease electrical performance, and complicate the manufacturing process (Brief, pages 7-8; Reply Brief, pages 3-4). Appellants state that the negative impact of adding bond wires to the flip chip package in Farnworth is based on structural aspects of bond wires "which are widely documented and well known to those of ordinary skill in the art." Reply Brief, page 3.

Appellants' arguments are not persuasive. The arguments of appellants' attorney cannot take the place of evidence lacking in the record. *See In re Scarborough,* 500 F.2d 560, 566, 182 USPQ

298, 302 (CCPA 1974); *In re Lindner*, 457 F.2d 506, 508, 173 USPQ 356, 358 (CCPA 1972). Appellants have not, on this record, substantiated their argument that the negative impact of adding bond wires is "widely documented and well known" in the art. In contrast, the examiner has shown evidence of the similarity in structures and purpose of Farnworth and Lee, as well as motivation to modify the structure of Farnworth, i.e., the advantages taught by Lee for the lead on chip (LOC) package (Answer, paragraph bridging pages 4-5 and pages 6-7). *See In re Mayne*, 104 F.3d 1339, 1342, 41 USPQ2d 1451, 1454 (Fed. Cir. 1997) ("When relying on numerous references or a modification of prior art, it is incumbent upon the examiner to identify some suggestion to combine references or make the modification. [Citations omitted]."). We determine that the examiner has met the initial burden of establishing a case of *prima facie* obviousness for reasons discussed above. We note that appellants have not challenged or contested the examiner's showing of motivation or suggestion of modification (i.e., the advantages taught by Lee). Appellants have only presented unsupported arguments concerning the negative impact of the proposed modification.

Appellants argue that the combination of Farnworth and Lee does not teach or suggest the claim limitations of claims 3, 6, 11, 12 and 14 (Brief, page 9). This argument is not persuasive since the applied references disclose the adhesive-coated polyimide tape recited in claim 3 on appeal (e.g., see Lee, col. 4, ll. 60-63), the lead fingers of the conductive traces as recited in claim 6 on appeal (e.g., see Farnworth, col. 4, ll. 33-38), and the thermocompression bonds of claims 11 and 12 on appeal (e.g., see Lee, col. 4, ll. 65-67). Furthermore, Lee teaches external connection means exposed for electrical connection to the external interconnections (col. 5, ll. 21-24), and thus would have suggested any conductive element such as a conductive polymer as recited in claim 14 on appeal that would suffice for the external connection.

For the foregoing reasons and those stated in the Answer, we determine that the examiner has established a *prima facie* case of obviousness in view of the reference evidence. Based on the totality of the record, including due consideration of appellants' arguments, we determine that the preponderance of evidence weighs most heavily in favor of obviousness within the meaning of section 103(a). *See In re Oetiker*, 977 F.2d 1443, 1445, 24 USPQ2d 1443, 1444 (Fed. Cir. 1992). Accordingly, we

affirm the examiner's rejection of claims 1 through 20 under 35 U.S.C. § 103(a) over Farnworth in view of Lee.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a)(iv)(effective Sep. 13, 2004; 69 Fed. Reg. 49960 (Aug. 12, 2004); 1286 Off. Gaz. Pat. Office 21 (Sep. 7, 2004)).

AFFIRMED

Thomas A. Waltz
Administrative Patent Judge)
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Romulo H. Delmendo) BOARD OF PATENT
Administrative Patent Judge) APPEALS
) AND
) INTERFERENCES
)
)
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TAW/tdl

Appeal No. 2004-2144
Application No. 09/483,712

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